# BE-S1000 Microprocessor
## Preliminary Datasheet

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## 1 Introduction

The BE-S1000 microprocessor is a *System-on-a-Chip* (**SoC**) for general purpose servers that require high performance, low power consumption, and multiple PCIe Gen4 interfaces with extensive customization options. It complies with Arm® Server Base System Architecture, IPMI, ACPI, and UEFI specifications.

The SoC implements 48 Arm Cortex™-A75 cores. Each core operates at 2 GHz and supports L1, L2, L3, and L4 coherent caches.

The BE-S1000 implements six independent DDR4-3200 memory channels and a wide range of peripheral interfaces: PCIe Gen4, 1 Gb Ethernet, USB 2.0, SPI, UART, GPIO, etc.

The SoC provides three PCIe Gen4 CCIX interfaces to build a multi-processor system up to four BE-S1000 microprocessors and with a joint L4 coherent cache.

The BE-S1000 complies with Arm TrustZone® technology and contains the capabilities necessary to build trusted systems.

## 1.1 Main Features

**Table 1-1 Main features**

| Feature | Description |
|---|---|
| **Armv8-A (v8.2) Architecture** | 48 Arm Cortex-A75 cores operating at 2 GHz |
| | 12 core clusters (4 cores and 2 MB L3 cache per cluster) |
| | 64 KB L1 instruction cache, 64 KB L1 data cache, and 512 KB L2 cache per core |
| **L4 Coherent Cache** | 32 MB L4 cache |
| **External Memory Interface** | Six 64-bit DRAM channels with support of DDR4-3200 and ECC |
| | Up to 768 GB per socket (128 GB per channel) |
| **Multi-SoC Interconnect** | Three CCIX interfaces x16, each lane operates with 16 Gb/s |
| **High Speed Peripherals** | 80 PCIe lanes of PCIe Gen4 (48 lanes are shared with CCIX interfaces) |
| | USB 2.0 ULPI interface |
| | Two 1 Gb Ethernet RGMII interfaces |
| **Low Speed Peripherals** | Four peripheral timers |
| | GPIOx32 |
| | Two UARTs |
| | QSPI |
| | Three $I^2C$/SMBus controllers |
| | Optionally: GPIOx16 or eSPI |
| | Optionally: GPIOx8 or QSPI |
| | Optionally: GPIOx8 or $I^2C$/SMBus + $I^2C$/SMBus + UART |
| **Security** | Arm TrustZone architecture |
| | Secure boot |
| **System Monitoring and Debug** | 24 PVT sensor blocks |
| | Watchdog timer |
| | Arm CoreSight™ debug and trace architecture |
| **Package** | FCLGA-3467 58x75.5 mm, 0.50 mm pitch, 3467 pins |
| **Power Consumption** | 120 W |
| **Operating Temperature** | From 0 to +70°C |
| **Technology** | TSMC 16FFC |

**NOTE:** The features in the table above are subject to change without notice.

## 1.2 Block Diagram

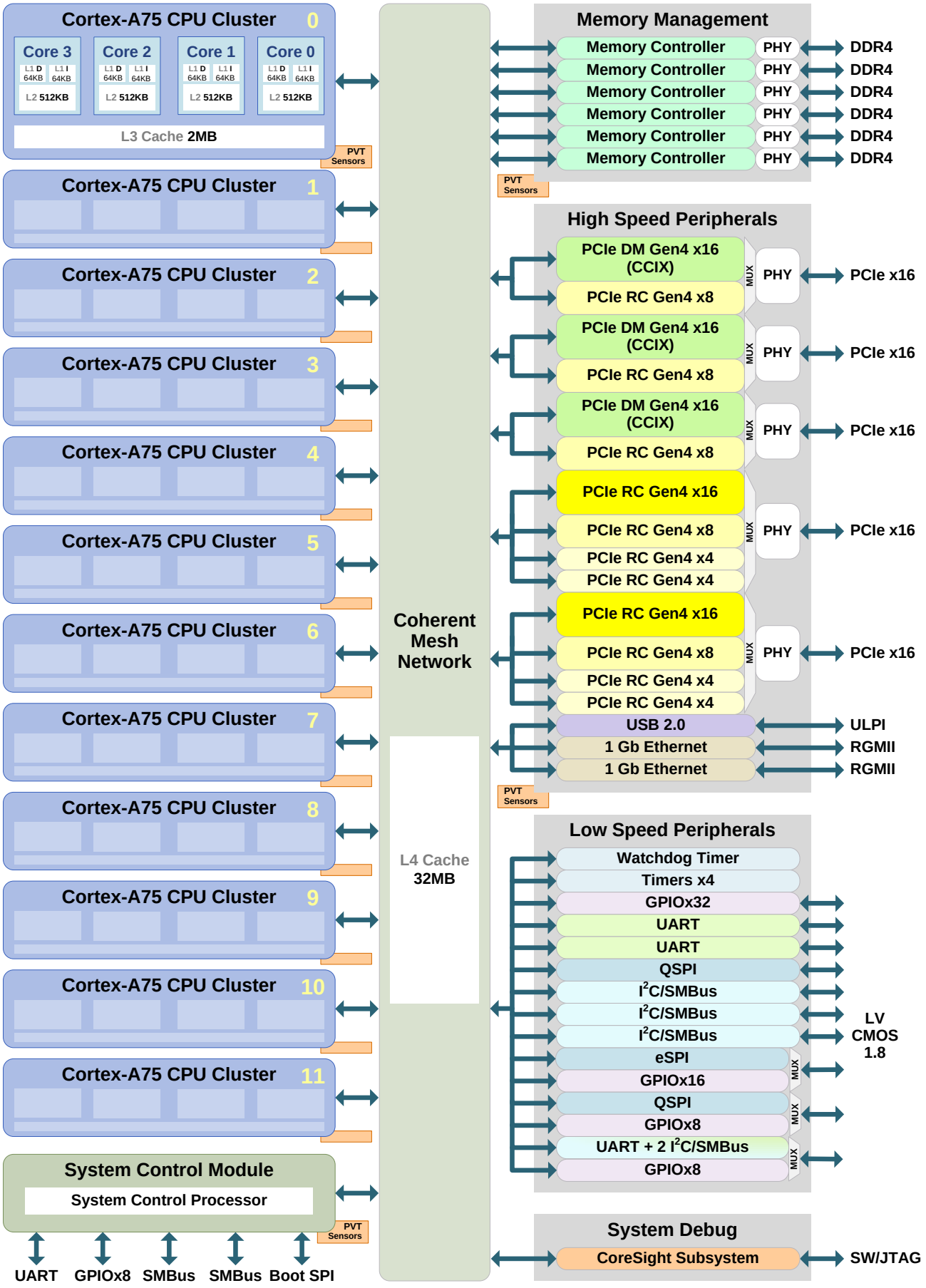



**Figure 1-1 Block diagram**

# 2 Detailed Description

## 2.1 Arm Cortex-A75 CPU Cluster

The SoC contains 48 Arm Cortex-A75 cores in 12 clusters.

Each cluster contains four cores (2 GHz) and L3 (2 MB) cache. Arm Cortex-A75 implements the Armv8-A (v8.2) architecture.

Each core contains 512 KB L2 cache, 64 KB L1 instruction cache, and 64 KB L1 data cache.

A core supports the following ISA extensions:

- CRC32
- SQRDMLAH and SQRDMLSH
- UDOT and SDOT
- LDADD, LDCLR, LDEOR, LDSET, LDSMAX, LDSMIN, LDUMAX, LDUMIN, CAS, CASP, and SWP
- DC CVAP
- DAPRB, LDAPRH, and LDAPR

None of the cores in the clusters include optional Arm Cortex-A75 core Cryptographic Extension.

A core can operate in one of two possible states, known as the secure and non-secure. By propagating the security state of the core through the on-chip interconnect to target-based transaction filters, the TrustZone technology is extended through the SoC architecture, creating a robust platform supporting fully isolated trusted and non-trusted worlds.

## 2.2 DDR4 Memory Subsystem

The BE-S1000 provides six memory channels. Each channel includes DDR4 memory controller and integrated *Physical Layer* (**PHY**), as shown in the following figure.

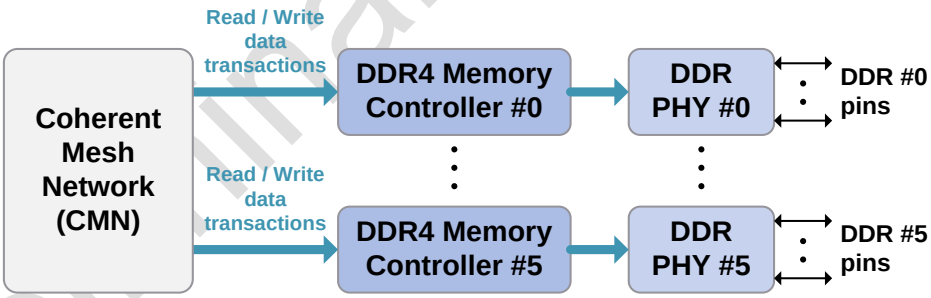



**Figure 2-1 DDR4 memory subsystem diagram**

Each memory channel supports:

- Up to 128 GB physical memory per channel
- 64-bit DDR4 (speed grades up to DDR4-3200)
- Integrated PHY
- Up to 4 memory ranks
- 1:2 frequency ratio mode
- 44-bit application address width
- 256-bit datawidth
- *Error Correction Code* (**ECC**): *Single Error Correction/Double Error Detection* (**SEC/DED**)

- DDR4U and DDR4L
- Industry standard UDIMMs and RDIMMs
- Low area, low power architecture
- Programmable support for 1T/2T memory command timing
- Software programmable *Quality of Service* (**QoS**)
- Automatic DDR4 low power mode operation
- Integrated PVT Controller

## 2.3 Coherent Mesh Network

*Coherent Mesh Network* (**CMN**) is based on the Arm CoreLink™ CMN-600. The CMN provides interconnection of the BE-S1000 macro-modules, manages the Level 4 coherent cache, and maps the global memory address space.

High-performance distributed system level cache (32 MB) includes an integrated *Point-of-Serialization* (**PoS**), *Point-of-Coherency* (**PoC**), and its **SLC** (also referred to as *Agile System Cache*), can be used both for compute and *Input/Output* (**I/O**) caching.

The CMN provides the following key features:

- 6×6 mesh network topology
- Pair of 256-bit data channels, one for each direction
- High-performance distributed SLC and *Snoop Filter* (**SF**)
- DVM message transport between masters
- Programmable *System Address Map* (**SAM**)
- RAS features including transport parity, optional data path parity, SEC/DED, ECC, and data poisoning signaling
- Supports CCIX links for coherent communication
- QoS regulation for shaping traffic profiles
- Performance monitoring events
- Separate caches for secure and non-secure transactions

## 2.4 System Control Module

This module is used to manage all the SoC subsystems.

It contains the following main blocks:

- *System Control Processor* (**SCP**) supports the following service functions:
  - The SoC startup
  - Initial configuration of all the SoC modules
  - SoC's state monitoring
- Boot SPI controller for initial boot
- UART, GPIOx8, and two $I^2C$/SMBus interfaces used for system control functions

  **NOTE:** These interfaces are under SCP control and are not available for Arm Cortex A-75 cores. The interfaces can be used if they have special support from the SDK.

## 2.5 High Speed Peripherals

BE-S1000 provides the following types of high speed interfaces:

- PCIe interfaces
- USB 2.0
- 1 Gb Ethernet

### *2.5.1 PCIe Interfaces*

BE-S1000 provides 80 PCIe lanes of PCIe Gen4 that are shared out for three PCIe DM x16 Gen4 controllers and eleven PCIe RC Gen4 controllers.

The PCIe controllers are combined into five *Macro-Modules* (**MM**). Each MM is connected to the Coherent Mesh Network and supports 16 physical interface lanes through four integrated PCIe PHYs x4.

The following figure shows main functional subsystems of each PCIe MM.

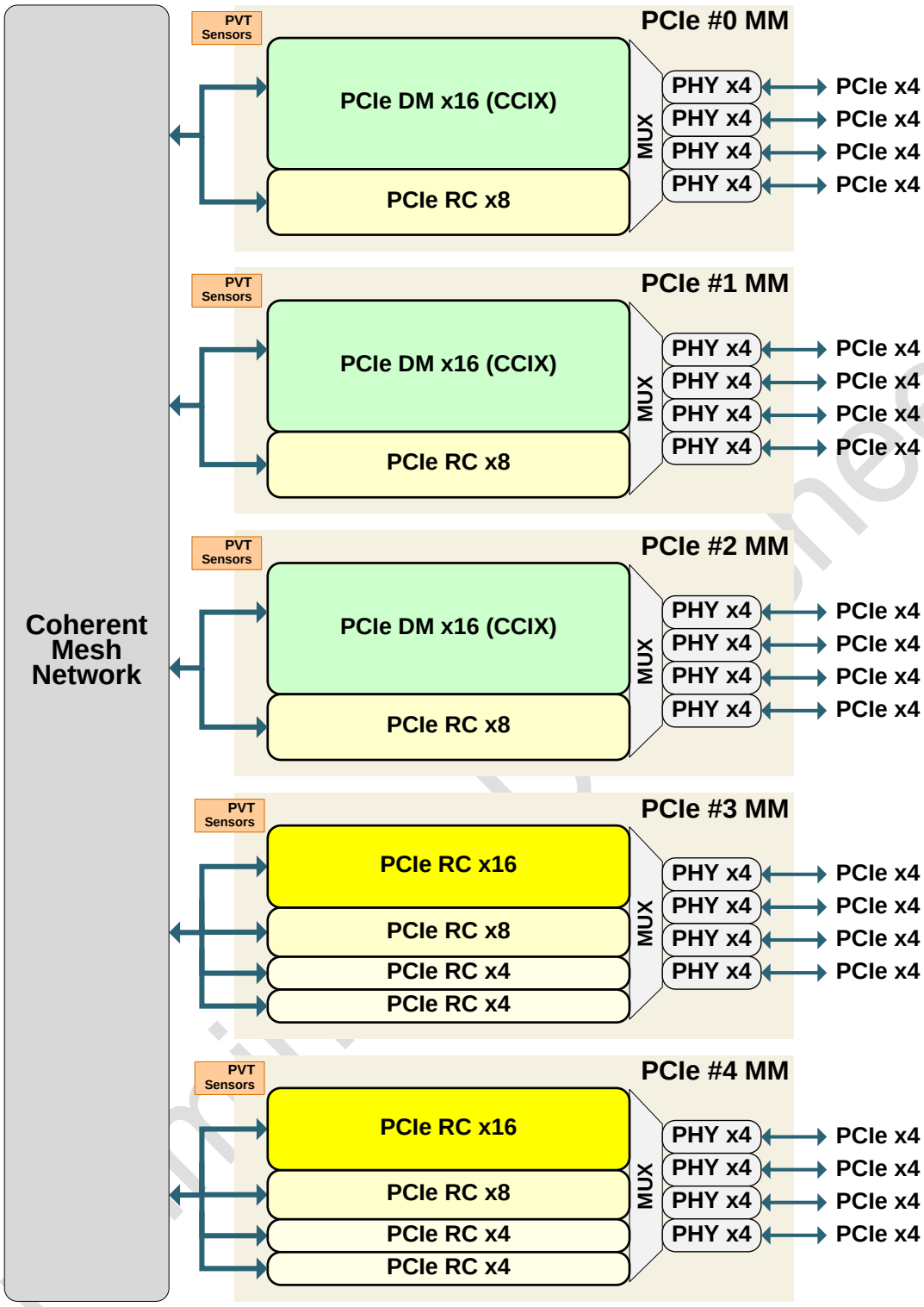



**Figure 2-2 PCIe macro-modules**

As the figure above shows, PCIe controllers of each macro-module can operate through up to 16 lanes.

Each PCIe MM contains software controlled registers to provide the multiplexing function of PCIe PHYs.

> **NOTE**: For details on how to control multiplexing PCIe PHYs, refer to section ***5 LCRU Implementations in Macro-Modules*** in ***BE-S1000 PROGRAMMING GUIDE Vol.6.1 System Monitoring and Management. Local Clock and Reset Unit (LCRU)***.

The following table shows possible PCIe layouts in BE-S1000.

**Table 2-1 Possible PCIe layouts**

| PHY | Option | Controller | Operational mode | Lane count |
|---|---|---|---|---|
| PCIe x16 #0, #1, or #2 | 1 | PCIe DM x16 (CCIX) | PCIe CCIX x16 | 16 |
| | | PCIe RC x8 | not used | 0 |
| | 2 | PCIe DM x16 (CCIX) | PCIe RC x16 | 16 |
| | | PCIe RC x8 | not used | 0 |
| | 3 | PCIe DM x16 (CCIX) | PCIe EP x16 | 16 |
| | | PCIe RC x8 | not used | 0 |
| | 4 | PCIe DM x16 (CCIX) | PCIe RC x8 | 8 |
| | | PCIe RC x8 | PCIe RC x8 | 8 |
| | 5 | PCIe DM x16 (CCIX) | PCIe EP x8 | 8 |
| | | PCIe RC x8 | PCIe RC x8 | 8 |
| PCIe x16 #3 or #4 | 1 | PCIe RC x16 | PCIe RC x16 | 16 |
| | | PCIe RC x8 | not used | 0 |
| | | PCIe RC x4 | not used | 0 |
| | | PCIe RC x4 | not used | 0 |
| | 2 | PCIe RC x16 | PCIe RC x8 | 8 |
| | | PCIe RC x8 | PCIe RC x8 | 8 |
| | | PCIe RC x4 | not used | 0 |
| | | PCIe RC x4 | not used | 0 |
| | 3 | PCIe RC x16 | PCIe RC x8 | 8 |
| | | PCIe RC x8 | not used | 0 |
| | | PCIe RC x4 | PCIe RC x4 | 4 |
| | | PCIe RC x4 | PCIe RC x4 | 4 |
| | 4 | PCIe RC x16 | not used | 0 |
| | | PCIe RC x8 | PCIe RC x8 | 8 |
| | | PCIe RC x4 | PCIe RC x4 | 4 |
| | | PCIe RC x4 | PCIe RC x4 | 4 |
| | 5 | PCIe RC x16 | PCIe RC x4 | 4 |
| | | PCIe RC x8 | PCIe RC x4 | 4 |
| | | PCIe RC x4 | PCIe RC x4 | 4 |
| | | PCIe RC x4 | PCIe RC x4 | 4 |

#### *2.5.1.1 PCIe RC Gen4*

The SoC contains eleven PCIe *Root Complex* (**RC**) Gen4 subsystems:

- Two PCIe x16
- Five PCIe x8
- Four PCIe x4

Each PCIe RC subsystem contains PCIe controller, PCS, and integrated PHY. The controller supports all non-optional features of the ***PCI Express Base Specification, Revision 4.0, Version 1.0***.

Each PCIe RC subsystem provides the following main features:

- Up to 16.0 GT/s (~ 2 GB/s) per single lane

- PCIe *Active State Power Management* (**ASPM**)
- PCIe *Advanced Error Reporting* (**AER**) with multiple header logging
- *Internal Address Translation Unit* (**IATU**)
- Embedded multichannel DMA controller
- Automatic lane reversal
- ECRC generation and checking
- Quality of service
- Virtual channels:
    - 1 channel for PCIe x4
    - 2 channels for PCIe x8
    - 3 channels for PCIe x16
- Maximum payload size:
    - 256 bytes for PCIe x4
    - 512 bytes for PCIe x8
    - 512 bytes for PCIe x16

Each subsystem can work both in secure and non-secure modes.

#### *2.5.1.2 PCIe DM x16 Gen4*

The SoC contains three PCIe *Dual Mode* (**DM**) x16 Gen4 subsystems.

Each PCIe DM subsystem contains PCIe controller, PCS, and integrated PHY. The controller supports all non-optional features of the ***PCI Express Base Specification, Revision 4.0, Version 1.0***.

Each PCIe DM subsystem supports the following main features:

- Transfer rates up to 16.0 GT/s (~ 2 GB/s) per single lane
- CCIX transport protocol
- Optimized CCIX TLP interface
- Embedded CXS controller that supports *Coherent Multichip Link* (**CML**)
- PCIe *Active State Power Management* (**ASPM**)
- PCIe *Advanced Error Reporting* (**AER**) with multiple header logging
- *Internal Address Translation Unit* (**IATU**)
- Embedded multichannel DMA controller
- Automatic lane reversal
- ECRC generation and checking
- Integrated MSI reception module
- Quality of service
- 2 virtual channels
- Maximum payload size 1024 bytes

The subsystem provides capability of building a multi-socket system with up to four BE-S1000 microprocessors and a joint coherent cache L4. For more details, see Multi-socket Systems.

Each subsystem can work both in secure and non-secure modes.

#### *2.5.1.3 Multi-socket Systems*

BE-S1000 contains three PCIe DM Gen4 subsystems that provide capability of building a multi-processor system with up to four BE-S1000 microprocessors and a joint coherent cache L4.

Each PCIe DM Gen4 subsystem supports CCIX Transport Protocol and contains embedded CXS controller that supports *Coherent Multichip Link* (**CML**).

The following diagram shows an example of PCIe CCIX subsystem configuration that can be used to build a two-socket *Printed Circuit Board* (**PCB**).

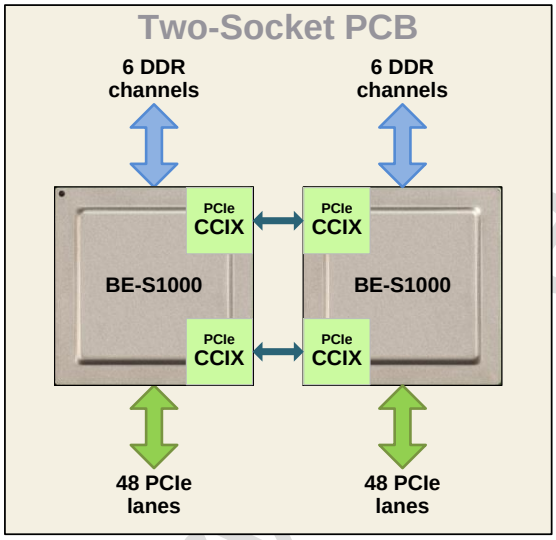



**Figure 2-3 Two-socket BE-S1000 system on a PCB**

The following diagram shows an example of PCIe CCIX subsystem configuration that can be used to build a four-socket PCB.

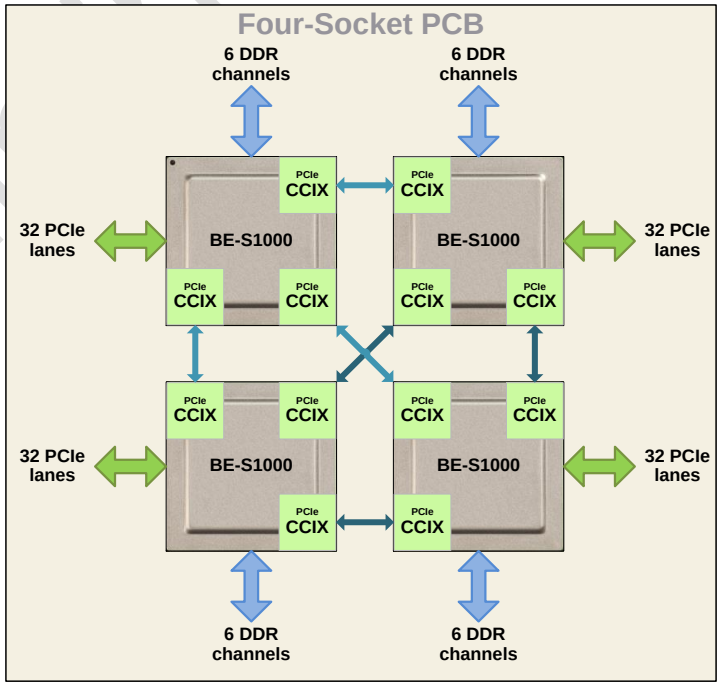



**Figure 2-4 Four-socket BE-S1000 system on a PCB**

### 2.5.2 USB 2.0

The USB 2.0 controller is compatible with the ***xHCI Specification*** by Intel Corporation. The output interface is compliant with ***UTMI+ Low Pin Interface (ULPI) Specification***.

The controller contains one port optimized for high-bandwidth applications. It supports the following device types:

- High-Speed up to 480 Mbps
- Full-Speed up to 12 Mbps
- Low-Speed up to 1.5 Mbps

It can work both in secure and non-secure modes.

### 2.5.3 1 Gb Ethernet

There are two identical *1 Gigabit Media Access Controllers* (**GMAC**) in the SoC.

Each controller enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard.

GMAC provides the following main features:

- RGMII interface
- 10, 100, and 1000 Mbps modes
- Full-duplex and half-duplex operation support
- Embedded DMA controller with independent transmit and receive engines

Each controller can work both in secure and non-secure modes.

## 2.6 Low Speed Peripherals

The BE-S1000 *Low Speed Peripherals* (**LSP**) subsystem contains Watchdog Timer and four peripheral Timers and the following interfaces:

- General purpose input/output (GPIO) with up to 32, 16, 8, and 8 bits of I/O
- Up to 2 universal asynchronous receivers/transmitters (UART)
- Up to 2 quad serial peripheral interfaces (QSPI)
- Enhanced Serial Peripheral Interface (eSPI)
- Up to 5 inter-integrated circuits/system management bus controller ($I^2C$/SMBus)

The subsystem is connected to the Coherent Mesh Network and can operate under control of application processor (a core of Arm Cortex-A75 clusters) or SCP.

The following diagram shows main controllers of the LSP subsystem.

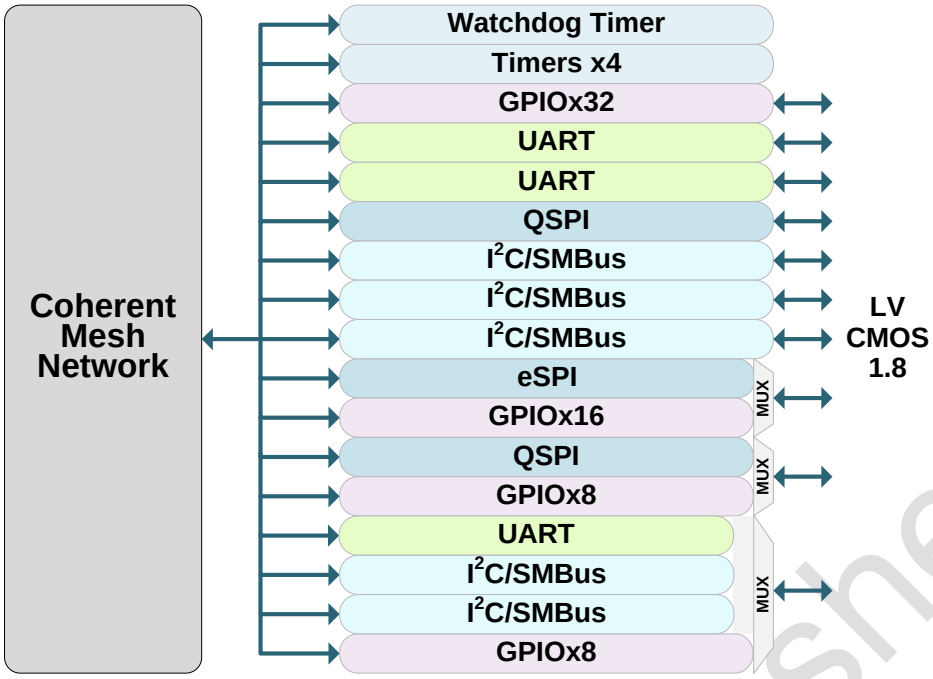



**Figure 2-5 Low speed peripherals**

As the figure above shows, some LSP controllers share physical interfaces: 32 pins of the SoC can be used for eight LSPs.

LSP subsystem contains software controlled registers to provide the function of multiplexing physical interfaces.

As shown in the following figure, System Control Module contains programmable register, used to control the LSP interface multiplexer.

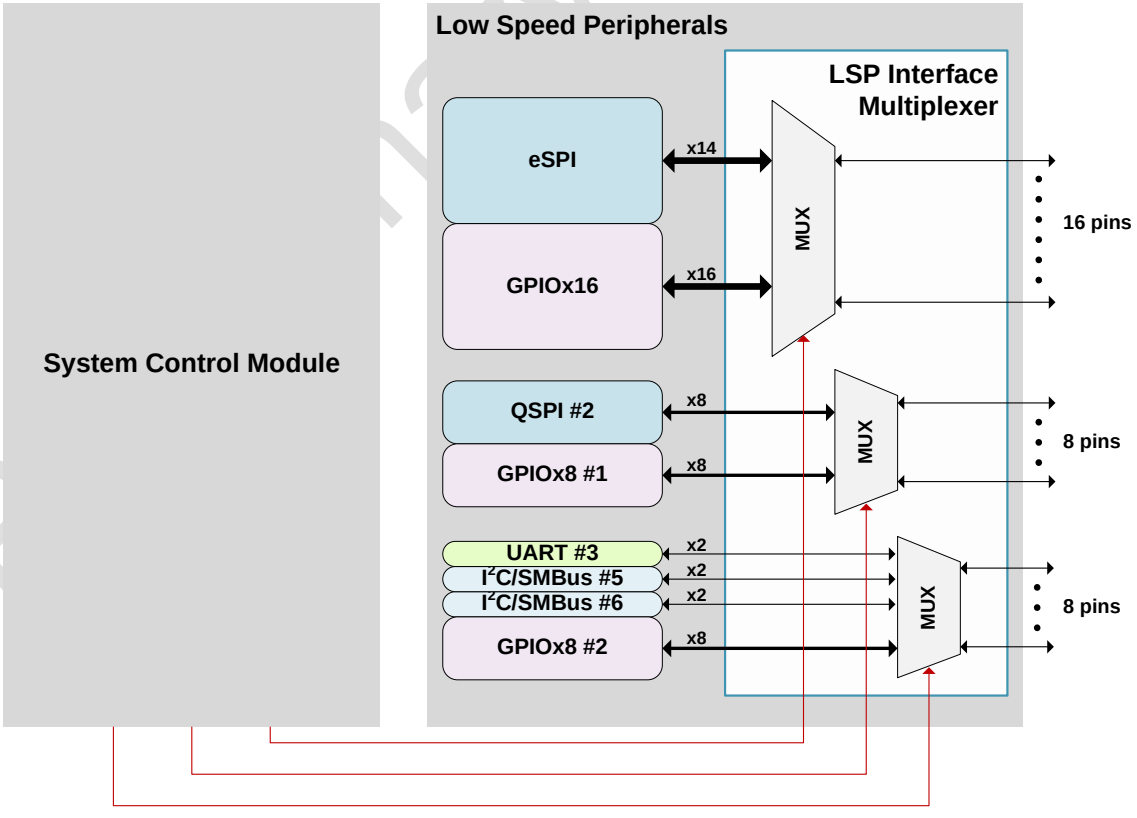



**Figure 2-6 LSP multiplexing control**

**NOTE:** For detailed LSP configuration description, refer to section ***5.6 SC MM LCRU*** in ***BE-S1000 PROGRAMMING GUIDE Vol.6.1 System Monitoring and Management. Local Clock and Reset Unit (LCRU)***.

The following table shows possible LSP layouts in BE-S1000.

**Table 2-2 Possible layouts for LSP**

| Pin port | Option | Interface | Pin count |
|---|---|---|---|
| x16 | 1 | eSPI (SSx2) | 14 |
| | | GPIO x16 | not used |
| | 2 | eSPI (SSx2) | not used |
| | | GPIO x16 | 16 |
| x8 | 1 | QSPI (SSx4) | 8 |
| | | GPIO x8 | not used |
| | 2 | QSPI (SSx4) | not used |
| | | GPIO x8 | 8 |
| x8 | 1 | $I^2C$/SMBus | 2 |
| | | $I^2C$/SMBus | 2 |
| | | UART | 2 |
| | | GPIO x8 | not used |
| | 2 | $I^2C$/SMBus | not used |
| | | $I^2C$/SMBus | not used |
| | | UART | not used |
| | | GPIO x8 | 8 |

### 2.6.1 GPIO

The SoC provides up to 64 individually programmable *General Purpose Input/Output* (**GPIO**) pins.

The SoC contains four GPIO controllers that support correspondently up to 32, 16, 8, and 8 bits of I/O. For details on possible GPIO pin configurations, see corresponding table in Low Speed Peripherals.

Each GPIO controller controls the direction of data, data transactions, and interrupts on external pads using memory-mapped registers.

### 2.6.2 UART

There are three *Universal Asynchronous Receivers/Transmitters* (**UART**) in the SoC.

The first UART operates only in secure mode, the second one operates only in non-secure mode. The use of the third one is optional, it depends on LSP interface multiplexer. For details, see corresponding table in Low Speed Peripherals.

An UART contains registers that control:

- Character length
- Baud rates up to 1.5 Mbaud
- Parity generation/checking
- Interrupt generation

### 2.6.3 QSPI

There are two *Quad Serial Peripheral Interface* (**QSPI**) controllers in the SoC.

The QSPI controller is a full-duplex master synchronous serial interface used for short distance communication with up to two external slave SPI devices (SSx2). It supports Single/Dual/Quad SPI mode of operation.

A master (a core or DMA controller) accesses data, control, and status information on the QSPI controller through the APB interface.

The QSPI controller can connect to a serial-slave peripheral device using ***Motorola SPI interface***.

### *2.6.4 eSPI*

The *Enhanced Serial Peripheral Interface* (**eSPI**) is a synchronous serial communication interface used for short distance communication.

Additional eSPI signals in comparison with SPI Interface:

- `RESET` programmable as input or output
- `ALERT` input interrupts

eSPI device communicates in full-duplex mode using master-slave architecture with up to four external slave SPI devices (SSx4). It supports single/dual/quad SPI mode of operation.

For details on how to use the eSPI, see corresponding table in Low Speed Peripherals.

### *2.6.5 I²C/SMBus*

The *Inter-Integrated Circuits/System Management Bus* (**I²C/SMBus**) is a two-wire interface through which various system components can communicate with each other and with the rest of the system. It is based on the principles of operation of the I²C bus.

The SoC includes five I²C/SMBus controllers:

- Three I²C/SMBus controllers support the `ALERT` and `SUSPEND` signals and have dedicated pins
- Two I²C/SMBus controllers do not support the `ALERT` and `SUSPEND` signals and can be connected to pinout, as described in corresponding table in Low Speed Peripherals

### *2.6.6 Timers*

The module contains four independent peripheral timers.

Each peripheral timer is a 32-bit programmable timer supporting “free-running” and “user-defined count” modes.

In “user-defined count” mode, a timer counts down from a programmed value and generates an interrupt when the count reaches zero. Timer interrupt can be detected even when the system bus clock is stopped.

## 2.7 System Monitoring and Debug

### *2.7.1 Process, Voltage, and Temperature (PVT) Sensors*

The SoC contains twenty four identical PVT sensor blocks used to monitor process, voltage, and temperature in CPU clusters, memory channels, PCIe subsystems, and the system control module.

Each PVT sensor blocks provides the following features:

- Measurement readiness is determined by polling data register or listening the interrupt line
- Programmable upper and lower threshold values for the measured PVT parameters to produce out-of-range interrupts
- Programmable timeout value for repetitive PVT parameters monitoring

### 2.7.2 Watchdog Timer

*Watchdog Timer* (**WDT**) is used to prevent system lockup that may be caused by software errors or hardware conflicts.

If a timeout occurs, the WDT can perform one of the following operations:

- Generates a system reset
- Firstly it generates an interrupt and waits the interrupt is cleared until a second timeout and then generates a system reset

The generated interrupt is passed to the *Generic Interrupt Controller* (**GIC**). The generated reset is passed to the SCM, which in turn generates a reset for the components in the system. The WDT may be reset independently of other subsystems.

### 2.7.3 CoreSight Subsystem

The CoreSight subsystem provides a standard implementation of the Arm Debug Interface for debug tools to work with *Serial Wire or JTAG* (**SW/JTAG**) debug port.

The subsystem supports the following methods of debugging the SoC:

- “External” debug – conventional debug through the SW/JTAG interface
- “Self-hosted” debug – conventional debug with the processor running using a debug monitor that resides in memory
- Logging of hardware and software events in a trace, recorded in memory

It can work both in secure and non-secure modes.

# 3 Electrical Specifications

**NOTE:** The power supply parameteres and reference clock requirements are subject to change without notice.

## 3.1 Power Supply Parameters

BE-S1000 requires six isolated voltage supplies and single unified ground supply, as shown in the following table.

**Table 3-1 BE-S1000 power domains**

| Supply type | Pin name | Voltage, V | Max power, W |
|---|---|---|---|
| Core supply | VDD | 0.9 ± 10% | 81 |
| 0.85V voltage supply | VDD_PCIE0_VP<br>VDD_PCIE1_VP<br>VDD_PCIE2_VP<br>VDD_PCIE3_VP<br>VDD_PCIE4_VP | 0.85 ± 10% | 8.5 |
| PLL supply | VDD_PLL | 1.8 ± 10% | 0.27 |
| DDR supply | VDDQ012<br>VDDQ345 | 1.2 ± 10% | 12 |
| DDR PLL supply | VDD_DDR_PLL | 1.8 ± 10% | 0.09 |
| 1.8V voltage supply | VDD_PCIE0_VPH<br>VDD_PCIE1_VPH<br>VDD_PCIE2_VPH<br>VDD_PCIE3_VPH<br>VDD_PCIE4_VPH<br>VDD_PVT<br>VDDIO | 1.8 ± 10% | 18 |
| Ground | VSS<br>VSSIO | 0 ± 10% | 0 |
| **Total** | | | ~120 |

## 3.2 External Clocking

### *3.2.1 Reference Clock Signals*

**Table 3-2 Reference clock signals**

| Clock signal | Pin name | Frequency, MHz |
|---|---|---|
| Reference clock | REFCLK | 25 or 100 |
| PCIe PHY reference clock | PCIE*n*_CLK*m*_DN*<br>PCIE*n*_CLK*m*_DP* | 100 |

* *n* – number of PCIe MM, *m* – number of PCIe PHY. For details, refer to PCIe Interfaces.

### 3.2.2 Reference Clock Requirements

#### 3.2.2.1 Reference Clock

**Table 3-3 Reference clock requirements**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Input frequency | - | 25 or 100* | - | MHz |
| Duty cycle | 45 | - | 55 | % |
| Lock time | - | - | 70 | us |
| Reset time | 1 | - | - | us |

* The REFCLK_SEL signal level must correspond to frequency value of reference clock. For details, refer to the corresponding Pin Description.

#### 3.2.2.2 PCIe PHY Reference Clock

Each PCIe subsystem contains four PCIe x4 PHYs. The PHYs require input reference clock signals, as shown in the following figure.

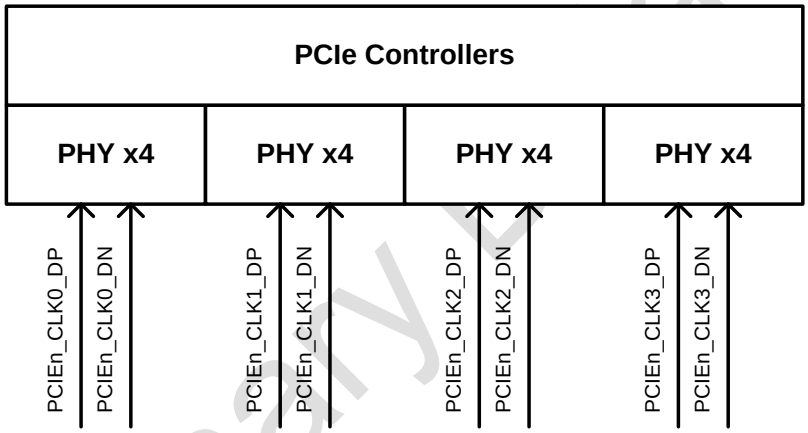



**Figure 3-1 PCIe PHY reference clock diagram**

The following table describes reference clock requirements for a PCIe PHY.

**Table 3-4 PCIe PHY reference clock requirements**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Input frequency | - | 100 | - | MHz |
| Rising edge rate | 0.6 | - | 4.0 | V/ns |
| Falling edge rate | 0.6 | - | 4.0 | V/ns |
| Average clock period accuracy | -300 | - | 2800 | ppm |
| Cycle to cycle jitter | - | - | 150 | ps |
| Duty cycle | 40 | - | 60 | % |
| Rise-fall matching | - | 20 | - | % |
| Clock source DC impedance | 40 | - | 60 | Ohms |

# 4 Power-Up/Down

## 4.1 Power-Up Sequence

The power-up sequence of power domains have to match the following recommendations. Any deviation from the following norms may cause:

- Overcurrent at start
- Incorrect device load
- Device damage

Requirements for the power-up:

1. Power domains must be enable when RESET_N, CS_TRST_N, PCIEx_PERST_N and TRST_N signals are active (active is low).
2. Supply power-up ramp rate for VDDQx and VDD_DDR_PLL is 5 mV/us max.
3. Supply ramp for others domains should be monotonic with a ramp time of no faster than 10 us and a rate no faster than (supply voltage)/10 us.
4. After 100 cycles of REFCLK reference clock (25 MHz), RESET_N signal must be high. CS_TRST_N and TRST_N signals must be high simultaneously with RESET_N.
5. Before 15 ms then RESET_N signal is high, PCIEx_PERST_N signals must be high.

The following figure shows the power-up sequence for BE-S1000.

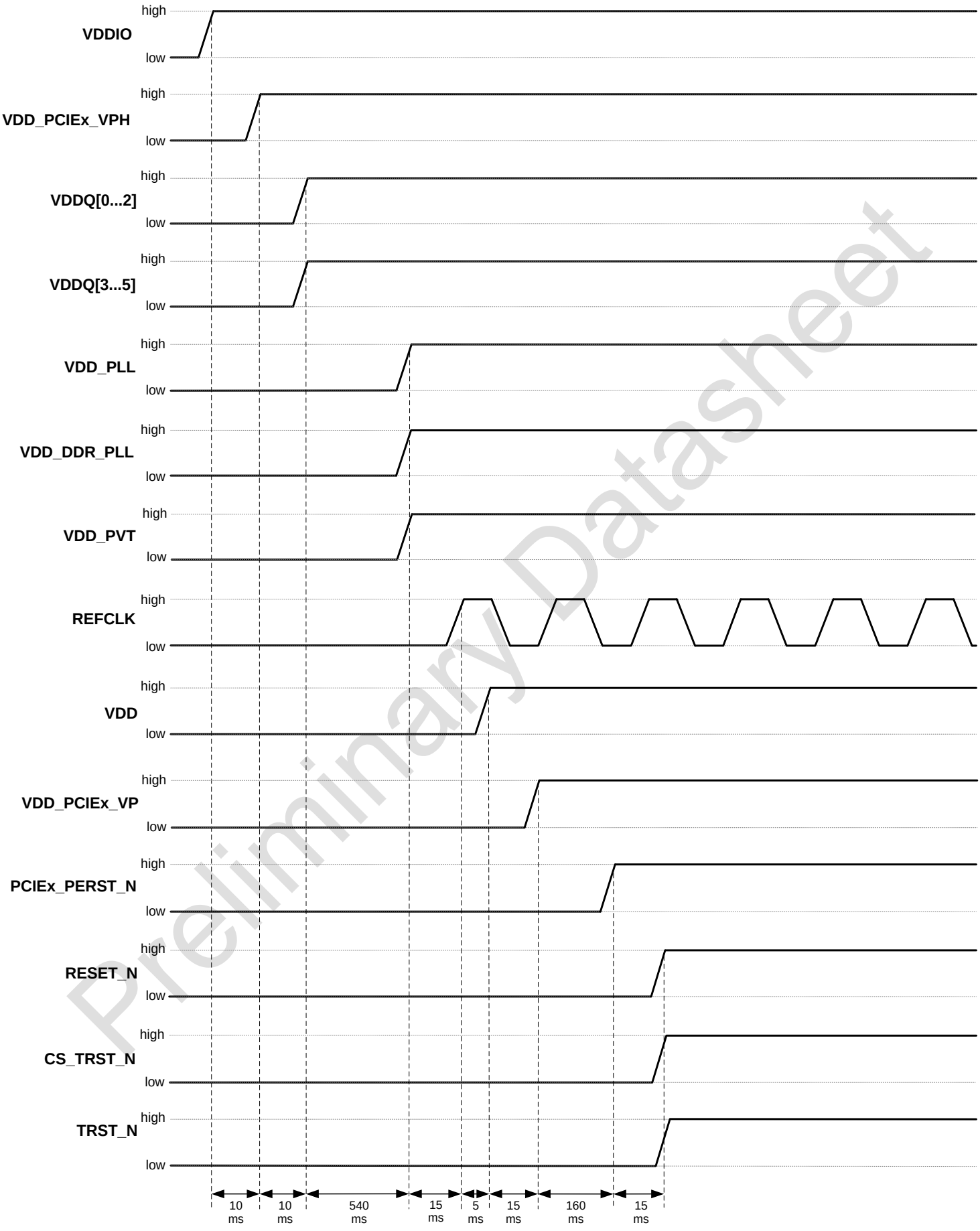



**Figure 4-1 Power-up sequence diagram for the BE-S1000**

## 4.2 Power-Down Sequence

Power-down must be done in reverse sequence given in 4.1 Power-Up Sequence

# 5 Pin Assignment

## 5.1 Pinout List

The following tables contain the list of I/O pins of the SoC including the power supply and ground pins. The following legend is applied for the following tables.

Legend:

| | |
|---|---|
| I | Input |
| O | Output |
| IO | Input/Output |
| A | Analog |
| P | Power supply |
| G | Ground |
| NC | Not connected |

### *5.1.1 DDR4*

#### *5.1.1.1 DDR #0*

**Table 5-1 DDR #0 pins**

| Pin name | Type | Description |
|---|---|---|
| DDR0_A[13:0] | O | SDRAM address |
| DDR0_A[14] | O | WE_N write enable |
| DDR0_A[15] | O | CAS_N column address strobe bus |
| DDR0_A[16] | O | RAS_N row address strobe bus |
| DDR0_A[17] | O | SDRAM address |
| DDR0_ACT_N | O | ACT_N activation command |
| DDR0_ALERT_N | IO | CRC or parity error<br>Indicates that a CRC or parity error has been detected for a previous command (active low) |
| DDR0_BA[1:0] | O | SDRAM bank address |
| DDR0_BG[1:0] | O | SDRAM bank group |
| DDR0_CKE[3:0] | O | SDRAM clock enable |
| DDR0_CLK_DN[3:0] | O | CLK0_C…CLK3_C SDRAM clock |
| DDR0_CLK_DP[3:0] | O | CLK0_T…CLK3_T SDRAM clock |
| DDR0_CS_N[3:0] | O | SDRAM chip select |
| DDR0_DQ[63:0] | IO | SDRAM data |
| DDR0_DQS_DN[0,2,4,6] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: DQS_n for byte; x16 mode: LDQS_n |
| DDR0_DQS_DN[1,3,5,7] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: DQS_n for byte; x16 mode: UDQS_n |
| DDR0_DQS_DN[8] | IO | SDRAM data strobe. x4 mode: DQS_n for ECC nibble; x8 mode: DQS_n for ECC byte; x16 mode: DQS_n for ECC byte |
| DDR0_DQS_DN[16:9] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: TDQS_n for byte; x16 mode: not used |
| DDR0_DQS_DN[17] | IO | SDRAM data strobe. x4 mode: DQS_n for ECC nibble; x8 mode: TDQS_n for ECC byte; x16 mode: not used |
| DDR0_DQS_DP[0,2,4,6] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DQS_p for byte; x16 mode: LDQS_p |

| Pin name | Type | Description |
|---|---|---|
| DDR0_DQS_DP[1,3,5,7] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DQS_p for byte; x16 mode: UDQS_p |
| DDR0_DQS_DP[8] | IO | SDRAM data strobe. x4 mode: DQS_p for ECC nibble; x8 mode: DQS_p for ECC byte; x16 mode: DQS_p for ECC byte |
| DDR0_DQS_DP[9,11,13,15] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DM/DBI/TDQS_p; x16 mode: DM/DBI for LDQ |
| DDR0_DQS_DP[10,12,14,16] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DM/DBI/TDQS_p; x16 mode: DM/DBI for UDQ |
| DDR0_DQS_DP[17] | IO | SDRAM data strobe. x4 mode: DQS_p for ECC nibble; x8 mode: DM/DBI/TDQS_p for ECC; x16 mode: DM/DBI for ECC |
| DDR0_DTO | O | Primary digital observation |
| DDR0_ECC[7:0] | IO | SDRAM data ECC |
| DDR0_ODT[3:0] | O | SDRAM on-die termination |
| DDR0_PAR | O | SDRAM parity value for DFI command |
| DDR0_RESET_N | O | SDRAM reset |
| DDR0_VREF | A | Reference voltage |
| DDR0_ZN | A | Calibration resistor connection |

#### *5.1.1.2 DDR #1*

**Table 5-2 DDR #1 pins**

| Pin name | Type | Description |
|---|---|---|
| DDR1_A[13:0] | O | SDRAM address |
| DDR1_A[14] | O | WE_N write enable |
| DDR1_A[15] | O | CAS_N column address strobe bus |
| DDR1_A[16] | O | RAS_N row address strobe bus |
| DDR1_A[17] | O | SDRAM address |
| DDR1_ACT_N | O | ACT_N activation command |
| DDR1_ALERT_N | IO | CRC or parity error<br>Indicates that a CRC or parity error has been detected for a previous command (active low) |
| DDR1_BA[1:0] | O | SDRAM bank address |
| DDR1_BG[1:0] | O | SDRAM bank group |
| DDR1_CKE[3:0] | O | SDRAM clock enable |
| DDR1_CLK_DN[3:0] | O | CLK0_C…CLK3_C SDRAM clock |
| DDR1_CLK_DP[3:0] | O | CLK0_T…CLK3_T SDRAM clock |
| DDR1_CS_N[3:0] | O | SDRAM chip select |
| DDR1_DQ[63:0] | IO | SDRAM data |
| DDR1_DQS_DN[0,2,4,6] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: DQS_n for byte; x16 mode: LDQS_n |
| DDR1_DQS_DN[1,3,5,7] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: DQS_n for byte; x16 mode: UDQS_n |
| DDR1_DQS_DN[8] | IO | SDRAM data strobe. x4 mode: DQS_n for ECC nibble; x8 mode: DQS_n for ECC byte; x16 mode: DQS_n for ECC byte |

| Pin name | Type | Description |
|---|---|---|
| DDR1_DQS_DN[16:9] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: TDQS_n for byte; x16 mode: not used |
| DDR1_DQS_DN[17] | IO | SDRAM data strobe. x4 mode: DQS_n for ECC nibble; x8 mode: TDQS_n for ECC byte; x16 mode: not used |
| DDR1_DQS_DP[0,2,4,6] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DQS_p for byte; x16 mode: LDQS_p |
| DDR1_DQS_DP[1,3,5,7] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DQS_p for byte; x16 mode: UDQS_p |
| DDR1_DQS_DP[8] | IO | SDRAM data strobe. x4 mode: DQS_p for ECC nibble; x8 mode: DQS_p for ECC byte; x16 mode: DQS_p for ECC byte |
| DDR1_DQS_DP[9,11,13,15] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DM/DBI/TDQS_p; x16 mode: DM/DBI for LDQ |
| DDR1_DQS_DP[10,12,14,16] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DM/DBI/TDQS_p; x16 mode: DM/DBI for UDQ |
| DDR1_DQS_DP[17] | IO | SDRAM data strobe. x4 mode: DQS_p for ECC nibble; x8 mode: DM/DBI/TDQS_p for ECC; x16 mode: DM/DBI for ECC |
| DDR1_DTO | O | Primary digital observation |
| DDR1_ECC[7:0] | IO | SDRAM data ECC |
| DDR1_ODT[3:0] | O | SDRAM on-die termination |
| DDR1_PAR | O | SDRAM parity value for DFI command |
| DDR1_RESET_N | O | SDRAM reset |
| DDR1_VREF | A | Reference voltage |
| DDR1_ZN | A | Calibration resistor connection |

#### *5.1.1.3 DDR #2*

**Table 5-3 DDR #2 pins**

| Pin name | Type | Description |
|---|---|---|
| DDR2_A[13:0] | O | SDRAM address |
| DDR2_A[14] | O | WE_N write enable |
| DDR2_A[15] | O | CAS_N column address strobe bus |
| DDR2_A[16] | O | RAS_N row address strobe bus |
| DDR2_A[17] | O | SDRAM address |
| DDR2_ACT_N | O | ACT_N activation command |
| DDR2_ALERT_N | IO | CRC or parity error<br>Indicates that a CRC or parity error has been detected for a previous command (active low) |
| DDR2_BA[1:0] | O | SDRAM bank address |
| DDR2_BG[1:0] | O | SDRAM bank group |
| DDR2_CKE[3:0] | O | SDRAM clock enable |
| DDR2_CLK_DN[3:0] | O | CLK0_C…CLK3_C SDRAM clock |
| DDR2_CLK_DP[3:0] | O | CLK0_T…CLK3_T SDRAM clock |
| DDR2_CS_N[3:0] | O | SDRAM chip select |
| DDR2_DQ[63:0] | IO | SDRAM data |

| Pin name | Type | Description |
|---|---|---|
| DDR2_DQS_DN[0,2,4,6] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: DQS_n for byte; x16 mode: LDQS_n |
| DDR2_DQS_DN[1,3,5,7] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: DQS_n for byte; x16 mode: UDQS_n |
| DDR2_DQS_DN[8] | IO | SDRAM data strobe. x4 mode: DQS_n for ECC nibble; x8 mode: DQS_n for ECC byte; x16 mode: DQS_n for ECC byte |
| DDR2_DQS_DN[16:9] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: TDQS_n for byte; x16 mode: not used |
| DDR2_DQS_DN[17] | IO | SDRAM data strobe. x4 mode: DQS_n for ECC nibble; x8 mode: TDQS_n for ECC byte; x16 mode: not used |
| DDR2_DQS_DP[0,2,4,6] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DQS_p for byte; x16 mode: LDQS_p |
| DDR2_DQS_DP[1,3,5,7] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DQS_p for byte; x16 mode: UDQS_p |
| DDR2_DQS_DP[8] | IO | SDRAM data strobe. x4 mode: DQS_p for ECC nibble; x8 mode: DQS_p for ECC byte; x16 mode: DQS_p for ECC byte |
| DDR2_DQS_DP[9,11,13,15] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DM/DBI/TDQS_p; x16 mode: DM/DBI for LDQ |
| DDR2_DQS_DP[10,12,14,16] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DM/DBI/TDQS_p; x16 mode: DM/DBI for UDQ |
| DDR2_DQS_DP[17] | IO | SDRAM data strobe. x4 mode: DQS_p for ECC nibble; x8 mode: DM/DBI/TDQS_p for ECC; x16 mode: DM/DBI for ECC |
| DDR2_DTO | O | Primary digital observation |
| DDR2_ECC[7:0] | IO | SDRAM data ECC |
| DDR2_ODT[3:0] | O | SDRAM on-die termination |
| DDR2_PAR | O | SDRAM parity value for DFI command |
| DDR2_RESET_N | O | SDRAM reset |
| DDR2_VREF | A | Reference voltage |
| DDR2_ZN | A | Calibration resistor connection |

#### *5.1.1.4 DDR #3*

**Table 5-4 DDR #3 pins**

| Pin name | Type | Description |
|---|---|---|
| DDR3_A[13:0] | O | SDRAM address |
| DDR3_A[14] | O | WE_N write enable |
| DDR3_A[15] | O | CAS_N column address strobe bus |
| DDR3_A[16] | O | RAS_N row address strobe bus |
| DDR3_A[17] | O | SDRAM address |
| DDR3_ACT_N | O | ACT_N activation command |
| DDR3_ALERT_N | IO | CRC or parity error<br>Indicates that a CRC or parity error has been detected for a previous command (active low) |
| DDR3_BA[1:0] | O | SDRAM bank address |
| DDR3_BG[1:0] | O | SDRAM bank group |
| DDR3_CKE[3:0] | O | SDRAM clock enable |

| Pin name | Type | Description |
|---|---|---|
| DDR3_CLK_DN[0] | O | CLK0_C…CLK3_C SDRAM clock |
| DDR3_CLK_DP[0] | O | CLK0_T…CLK3_T SDRAM clock |
| DDR3_CS_N[3:0] | O | SDRAM chip select |
| DDR3_DQ[63:0] | IO | SDRAM data |
| DDR3_DQS_DN[0,2,4,6] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: DQS_n for byte; x16 mode: LDQS_n |
| DDR3_DQS_DN[1,3,5,7] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: DQS_n for byte; x16 mode: UDQS_n |
| DDR3_DQS_DN[8] | IO | SDRAM data strobe. x4 mode: DQS_n for ECC nibble; x8 mode: DQS_n for ECC byte; x16 mode: DQS_n for ECC byte |
| DDR3_DQS_DN[16:9] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: TDQS_n for byte; x16 mode: not used |
| DDR3_DQS_DN[17] | IO | SDRAM data strobe. x4 mode: DQS_n for ECC nibble; x8 mode: TDQS_n for ECC byte; x16 mode: not used |
| DDR3_DQS_DP[0,2,4,6] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DQS_p for byte; x16 mode: LDQS_p |
| DDR3_DQS_DP[1,3,5,7] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DQS_p for byte; x16 mode: UDQS_p |
| DDR3_DQS_DP[8] | IO | SDRAM data strobe. x4 mode: DQS_p for ECC nibble; x8 mode: DQS_p for ECC byte; x16 mode: DQS_p for ECC byte |
| DDR3_DQS_DP[9,11,13,15] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DM/DBI/TDQS_p; x16 mode: DM/DBI for LDQ |
| DDR3_DQS_DP[10,12,14,16] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DM/DBI/TDQS_p; x16 mode: DM/DBI for UDQ |
| DDR3_DQS_DP[17] | IO | SDRAM data strobe. x4 mode: DQS_p for ECC nibble; x8 mode: DM/DBI/TDQS_p for ECC; x16 mode: DM/DBI for ECC |
| DDR3_DTO | O | Primary digital observation |
| DDR3_ECC[7:0] | IO | SDRAM data ECC |
| DDR3_ODT[3:0] | O | SDRAM on-die termination |
| DDR3_PAR | O | SDRAM parity value for DFI command |
| DDR3_RESET_N | O | SDRAM reset |
| DDR3_VREF | A | Reference voltage |
| DDR3_ZN | A | Calibration resistor connection |

#### *5.1.1.5 DDR #4*

**Table 5-5 DDR #4 pins**

| Pin name | Type | Description |
|---|---|---|
| DDR4_A[13:0] | O | SDRAM address |
| DDR4_A[14] | O | WE_N write enable |
| DDR4_A[15] | O | CAS_N column address strobe bus |
| DDR4_A[16] | O | RAS_N row address strobe bus |
| DDR4_A[17] | O | SDRAM address |
| DDR4_ACT_N | O | ACT_N activation command |

| Pin name | Type | Description |
|---|---|---|
| DDR4_ALERT_N | IO | CRC or parity error<br>Indicates that a CRC or parity error has been detected for a previous command (active low) |
| DDR4_BA[1:0] | O | SDRAM bank address |
| DDR4_BG[1:0] | O | SDRAM bank group |
| DDR4_CKE[3:0] | O | SDRAM clock enable |
| DDR4_CLK_DN[3:0] | O | CLK0_C…CLK3_C SDRAM clock |
| DDR4_CLK_DP[3:0] | O | CLK0_T…CLK3_T SDRAM clock |
| DDR4_CS_N[3:0] | O | SDRAM chip select |
| DDR4_DQ[63:0] | IO | SDRAM data |
| DDR4_DQS_DN[0,2,4,6] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: DQS_n for byte; x16 mode: LDQS_n |
| DDR4_DQS_DN[1,3,5,7] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: DQS_n for byte; x16 mode: UDQS_n |
| DDR4_DQS_DN[8] | IO | SDRAM data strobe. x4 mode: DQS_n for ECC nibble; x8 mode: DQS_n for ECC byte; x16 mode: DQS_n for ECC byte |
| DDR4_DQS_DN[16:9] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: TDQS_n for byte; x16 mode: not used |
| DDR4_DQS_DN[17] | IO | SDRAM data strobe. x4 mode: DQS_n for ECC nibble; x8 mode: TDQS_n for ECC byte; x16 mode: not used |
| DDR4_DQS_DP[0,2,4,6] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DQS_p for byte; x16 mode: LDQS_p |
| DDR4_DQS_DP[1,3,5,7] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DQS_p for byte; x16 mode: UDQS_p |
| DDR4_DQS_DP[8] | IO | SDRAM data strobe. x4 mode: DQS_p for ECC nibble; x8 mode: DQS_p for ECC byte; x16 mode: DQS_p for ECC byte |
| DDR4_DQS_DP[9,11,13,15] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DM/DBI/TDQS_p; x16 mode: DM/DBI for LDQ |
| DDR4_DQS_DP[10,12,14,16] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DM/DBI/TDQS_p; x16 mode: DM/DBI for UDQ |
| DDR4_DQS_DP[17] | IO | SDRAM data strobe. x4 mode: DQS_p for ECC nibble; x8 mode: DM/DBI/TDQS_p for ECC; x16 mode: DM/DBI for ECC |
| DDR4_DTO | O | Primary digital observation |
| DDR4_ECC[7:0] | IO | SDRAM data ECC |
| DDR4_ODT[3:0] | O | SDRAM on-die termination |
| DDR4_PAR | O | SDRAM parity value for DFI command |
| DDR4_RESET_N | O | SDRAM reset |
| DDR4_VREF | A | Reference voltage |
| DDR4_ZN | A | Calibration resistor connection |

#### *5.1.1.6 DDR #5*

**Table 5-6 DDR #5 pins**

| Pin name | Type | Description |
|---|---|---|
| DDR5_A[13:0] | O | SDRAM address |
| DDR5_A[14] | O | WE_N write enable |

| Pin name | Type | Description |
|---|---|---|
| DDR5_A[15] | O | CAS_N column address strobe bus |
| DDR5_A[16] | O | RAS_N row address strobe bus |
| DDR5_A[17] | O | SDRAM address |
| DDR5_ACT_N | O | ACT_N activation command |
| DDR5_ALERT_N | IO | CRC or parity error<br>Indicates that a CRC or parity error has been detected for a previous command (active low) |
| DDR5_BA[1:0] | O | SDRAM bank address |
| DDR5_BG[1:0] | O | SDRAM bank group |
| DDR5_CKE[3:0] | O | SDRAM clock enable |
| DDR5_CLK_DN[3:0] | O | CLK0_C…CLK3_C SDRAM clock |
| DDR5_CLK_DP[3:0] | O | CLK0_T…CLK3_T SDRAM clock |
| DDR5_CS_N[3:0] | O | SDRAM chip select |
| DDR5_DQ[63:0] | IO | SDRAM data |
| DDR5_DQS_DN[0,2,4,6] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: DQS_n for byte; x16 mode: LDQS_n |
| DDR5_DQS_DN[1,3,5,7] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: DQS_n for byte; x16 mode: UDQS_n |
| DDR5_DQS_DN[8] | IO | SDRAM data strobe. x4 mode: DQS_n for ECC nibble; x8 mode: DQS_n for ECC byte; x16 mode: DQS_n for ECC byte |
| DDR5_DQS_DN[16:9] | IO | SDRAM data strobe. x4 mode: DQS_n for nibble; x8 mode: TDQS_n for byte; x16 mode: not used |
| DDR5_DQS_DN[17] | IO | SDRAM data strobe. x4 mode: DQS_n for ECC nibble; x8 mode: TDQS_n for ECC byte; x16 mode: not used |
| DDR5_DQS_DP[0,2,4,6] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DQS_p for byte; x16 mode: LDQS_p |
| DDR5_DQS_DP[1,3,5,7] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DQS_p for byte; x16 mode: UDQS_p |
| DDR5_DQS_DP[8] | IO | SDRAM data strobe. x4 mode: DQS_p for ECC nibble; x8 mode: DQS_p for ECC byte; x16 mode: DQS_p for ECC byte |
| DDR5_DQS_DP[9,11,13,15] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DM/DBI/TDQS_p; x16 mode: DM/DBI for LDQ |
| DDR5_DQS_DP[10,12,14,16] | IO | SDRAM data strobe. x4 mode: DQS_p for nibble; x8 mode: DM/DBI/TDQS_p; x16 mode: DM/DBI for UDQ |
| DDR5_DQS_DP[17] | IO | SDRAM data strobe. x4 mode: DQS_p for ECC nibble; x8 mode: DM/DBI/TDQS_p for ECC; x16 mode: DM/DBI for ECC |
| DDR5_DTO | O | Primary digital observation |
| DDR5_ECC[7:0] | IO | SDRAM data ECC |
| DDR5_ODT[3:0] | O | SDRAM on-die termination |
| DDR5_PAR | O | SDRAM parity value for DFI command |
| DDR5_RESET_N | O | SDRAM reset |
| DDR5_VREF | A | Reference voltage |
| DDR5_ZN | A | Calibration resistor connection |

### 5.1.2 High Speed Peripherals

#### 5.1.2.1 PCIe x16 #0

**Table 5-7 PCIe x16 #0 pins**

| Pin name | Type | Description |
|---|---|---|
| PCIE0_ATT_BUT[1:0] | I | Sets whether the system attention button is pressed |
| PCIE0_ATT_IND[3:0] | O | Controls the system attention indicator |
| PCIE0_CLK0_DN | I | PCIe differential reference clock |
| PCIE0_CLK0_DP | I | PCIe differential reference clock |
| PCIE0_CLK1_DN | I | PCIe differential reference clock |
| PCIE0_CLK1_DP | I | PCIe differential reference clock |
| PCIE0_CLK2_DN | I | PCIe differential reference clock |
| PCIE0_CLK2_DP | I | PCIe differential reference clock |
| PCIE0_CLK3_DN | I | PCIe differential reference clock |
| PCIE0_CLK3_DP | I | PCIe differential reference clock |
| PCIE0_CMD_INT[1:0] | I | Hot-plug controller command completed interrupt |
| PCIE0_INTRL_CTRL[1:0] | O | Electromechanical interlock control |
| PCIE0_INTRL_ENG[1:0] | I | System electromechanical interlock engaged |
| PCIE0_MRL_SENS[1:0] | I | MRL sensor state |
| PCIE0_PERST_N[1:0] | I | PERST |
| PCIE0_PRES_ST[1:0] | I | Presence detect state |
| PCIE0_PWR_CTRL[1:0] | O | Controls the system power controller |
| PCIE0_PWR_FAULT[1:0] | I | Power fault detected |
| PCIE0_PWR_IND[3:0] | O | Controls the system power indicator |
| PCIE0_RESREF | A | Reference resistor connection |
| PCIE0_RX_DN[15:0] | I | PCIe differential receive pair |
| PCIE0_RX_DP[15:0] | I | PCIe differential receive pair |
| PCIE0_TX_DN[15:0] | O | PCIe differential transmit pair |
| PCIE0_TX_DP[15:0] | O | PCIe differential transmit pair |

#### 5.1.2.2 PCIe x16 #1

**Table 5-8 PCIe x16 #1 pins**

| Pin name | Type | Description |
|---|---|---|
| PCIE1_ATT_BUT[1:0] | I | Sets whether the system attention button is pressed |
| PCIE1_ATT_IND[3:0] | O | Controls the system attention indicator |
| PCIE1_CLK0_DN | I | PCIe differential reference clock |
| PCIE1_CLK0_DP | I | PCIe differential reference clock |
| PCIE1_CLK1_DN | I | PCIe differential reference clock |

| Pin name | Type | Description |
|---|---|---|
| PCIE1_CLK1_DP | I | PCIe differential reference clock |
| PCIE1_CLK2_DN | I | PCIe differential reference clock |
| PCIE1_CLK2_DP | I | PCIe differential reference clock |
| PCIE1_CLK3_DN | I | PCIe differential reference clock |
| PCIE1_CLK3_DP | I | PCIe differential reference clock |
| PCIE1_CMD_INT[1:0] | I | Hot-plug controller command completed interrupt |
| PCIE1_INTRL_CTRL[1:0] | O | Electromechanical interlock control |
| PCIE1_INTRL_ENG[1:0] | I | System electromechanical interlock engaged |
| PCIE1_MRL_SENS[1:0] | I | MRL sensor state |
| PCIE1_PERST_N[1:0] | I | PERST |
| PCIE1_PRES_ST[1:0] | I | Presence detect state |
| PCIE1_PWR_CTRL[1:0] | O | Controls the system power controller |
| PCIE1_PWR_FAULT[1:0] | I | Power fault detected |
| PCIE1_PWR_IND[3:0] | O | Controls the system power indicator |
| PCIE1_RESREF | A | Reference resistor connection |
| PCIE1_RX_DN[15:0] | I | PCIe differential receive pair |
| PCIE1_RX_DP[15:0] | I | PCIe differential receive pair |
| PCIE1_TX_DN[15:0] | O | PCIe differential transmit pair |
| PCIE1_TX_DP[15:0] | O | PCIe differential transmit pair |

#### *5.1.2.3 PCIe x16 #2*

**Table 5-9 PCIe x16 #2 pins**

| Pin name | Type | Description |
|---|---|---|
| PCIE2_ATT_BUT[1:0] | I | Sets whether the system attention button is pressed |
| PCIE2_ATT_IND[3:0] | O | Controls the system attention indicator |
| PCIE2_CLK0_DN | I | PCIe differential reference clock |
| PCIE2_CLK0_DP | I | PCIe differential reference clock |
| PCIE2_CLK1_DN | I | PCIe differential reference clock |
| PCIE2_CLK1_DP | I | PCIe differential reference clock |
| PCIE2_CLK2_DN | I | PCIe differential reference clock |
| PCIE2_CLK2_DP | I | PCIe differential reference clock |
| PCIE2_CLK3_DN | I | PCIe differential reference clock |
| PCIE2_CLK3_DP | I | PCIe differential reference clock |
| PCIE2_CMD_INT[1:0] | I | Hot-plug controller command completed interrupt |
| PCIE2_INTRL_CTRL[1:0] | O | Electromechanical interlock control |
| PCIE2_INTRL_ENG[1:0] | I | System electromechanical interlock engaged |

| Pin name | Type | Description |
|---|---|---|
| PCIE2_MRL_SENS[1:0] | I | MRL sensor state |
| PCIE2_PERST_N[1:0] | I | PERST |
| PCIE2_PRES_ST[1:0] | I | Presence detect state |
| PCIE2_PWR_CTRL[1:0] | O | Controls the system power controller |
| PCIE2_PWR_FAULT[1:0] | I | Power fault detected |
| PCIE2_PWR_IND[3:0] | O | Controls the system power indicator |
| PCIE2_RESREF | A | Reference resistor connection |
| PCIE2_RX_DN[15:0] | I | PCIe differential receive pair |
| PCIE2_RX_DP[15:0] | I | PCIe differential receive pair |
| PCIE2_TX_DN[15:0] | O | PCIe differential transmit pair |
| PCIE2_TX_DP[15:0] | O | PCIe differential transmit pair |

#### *5.1.2.4 PCIe x16 #3*

**Table 5-10 PCIe x16 #3 pins**

| Pin name | Type | Description |
|---|---|---|
| PCIE3_ATT_BUT[3:0] | I | Sets whether the system attention button is pressed |
| PCIE3_ATT_IND[7:0] | O | Controls the system attention indicator |
| PCIE3_CLK0_DN | I | PCIe differential reference clock |
| PCIE3_CLK0_DP | I | PCIe differential reference clock |
| PCIE3_CLK1_DN | I | PCIe differential reference clock |
| PCIE3_CLK1_DP | I | PCIe differential reference clock |
| PCIE3_CLK2_DN | I | PCIe differential reference clock |
| PCIE3_CLK2_DP | I | PCIe differential reference clock |
| PCIE3_CLK3_DN | I | PCIe differential reference clock |
| PCIE3_CLK3_DP | I | PCIe differential reference clock |
| PCIE3_CMD_INT[3:0] | I | Hot-plug controller command completed interrupt |
| PCIE3_INTRL_CTRL[3:0] | O | Electromechanical interlock control |
| PCIE3_INTRL_ENG[3:0] | I | System electromechanical interlock engaged |
| PCIE3_MRL_SENS[3:0] | I | MRL sensor state |
| PCIE3_PERST_N[3:0] | I | PERST |
| PCIE3_PRES_ST[3:0] | I | Presence detect state |
| PCIE3_PWR_CTRL[3:0] | O | Controls the system power controller |
| PCIE3_PWR_FAULT[3:0] | I | Power fault detected |
| PCIE3_PWR_IND[7:0] | O | Controls the system power indicator |
| PCIE3_RESREF | A | Reference resistor connection |
| PCIE3_RX_DN[15:0] | I | PCIe differential receive pair |

| Pin name | Type | Description |
|---|---|---|
| PCIE3_RX_DP[15:0] | I | PCIe differential receive pair |
| PCIE3_TX_DN[15:0] | O | PCIe differential transmit pair |
| PCIE3_TX_DP[15:0] | O | PCIe differential transmit pair |

#### *5.1.2.5 PCIe x16 #4*

**Table 5-11 PCIe x16 #4 pins**

| Pin name | Type | Description |
|---|---|---|
| PCIE4_ATT_BUT[3:0] | I | Sets whether the system attention button is pressed |
| PCIE4_ATT_IND[7:0] | O | Controls the system attention indicator |
| PCIE4_CLK0_DN | I | PCIe differential reference clock |
| PCIE4_CLK0_DP | I | PCIe differential reference clock |
| PCIE4_CLK1_DN | I | PCIe differential reference clock |
| PCIE4_CLK1_DP | I | PCIe differential reference clock |
| PCIE4_CLK2_DN | I | PCIe differential reference clock |
| PCIE4_CLK2_DP | I | PCIe differential reference clock |
| PCIE4_CLK3_DN | I | PCIe differential reference clock |
| PCIE4_CLK3_DP | I | PCIe differential reference clock |
| PCIE4_CMD_INT[3:0] | I | Hot-plug controller command completed interrupt |
| PCIE4_INTRL_CTRL[3:0] | O | Electromechanical interlock control |
| PCIE4_INTRL_ENG[3:0] | I | System electromechanical interlock engaged |
| PCIE4_MRL_SENS[3:0] | I | MRL sensor state |
| PCIE4_PERST_N[3:0] | I | PERST |
| PCIE4_PRES_ST[3:0] | I | Presence detect state |
| PCIE4_PWR_CTRL[3:0] | O | Controls the system power controller |
| PCIE4_PWR_FAULT[3:0] | I | Power fault detected |
| PCIE4_PWR_IND[7:0] | O | Controls the system power indicator |
| PCIE4_RESREF | A | Reference resistor connection |
| PCIE4_RX_DN[15:0] | I | PCIe differential receive pair |
| PCIE4_RX_DP[15:0] | I | PCIe differential receive pair |
| PCIE4_TX_DN[15:0] | O | PCIe differential transmit pair |
| PCIE4_TX_DP[15:0] | O | PCIe differential transmit pair |

#### *5.1.2.6 USB 2.0*

**Table 5-12 USB 2.0 pins**

| Pin name | Type | Description |
|---|---|---|
| USB2_CFG | I | Double data rate enable |

| Pin name | Type | Description |
|---|---|---|
| USB2_CLK | I | PHY input clock (60 MHz) |
| USB2_DAT[7:0] | IO | USB data |
| USB2_DIR | I | USB data direction control<br>Controls the direction of the bidirectional data bus |
| USB2_NXT | I | ULPI next data<br>Indicates when the PHY has accepted the current byte from the link |
| USB2_STP | O | ULPI stop data<br>The link asserts this signal for one clock cycle to stop the current data stream to the data bus |

#### *5.1.2.7 1 Gb Ethernet*

**Table 5-13 GMAC pins**

| Pin name | Type | Description |
|---|---|---|
| G0_GP_IN | I | General purpose input |
| G0_GP_OUT | O | General purpose output |
| G0_MDC | O | Management data clock (up to 2.5 MHz) |
| G0_MDIO | IO | Management data input/output |
| G0_RX_CLK | I | Receive reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode) |
| G0_RX_DAT[3:0] | I | Receive data |
| G0_RX_DEN | I | Receive data |
| G0_TX_CLK | O | Transmit reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode) |
| G0_TX_DAT[3:0] | O | Transmit data |
| G0_TX_DEN | O | Transmit data enable |
| G1_GP_IN | I | General purpose input |
| G1_GP_OUT | O | General purpose output |
| G1_MDC | O | Management data clock (up to 2.5 MHz) |
| G1_MDIO | IO | Management data input/output |
| G1_RX_CLK | I | Receive reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode) |
| G1_RX_DAT[0…3] | I | Receive data |
| G1_RX_DEN | I | Receive data |
| G1_TX_CLK | O | Transmit reference clock (125 MHz in 1 Gbps, 25 MHz in 100 Mbps, 2.5 MHz in 10 Mbps mode) |
| G1_TX_DAT[3:0] | O | Transmit data |
| G1_TX_DEN | O | Transmit data enable |

### 5.1.3 Low Speed Peripherals

#### 5.1.3.1 GPIOx32

**Table 5-14 GPIOx32 pins**

| Pin name | Type | Description |
|---|---|---|
| GPIO32[31:0] | IO | GPIO data |

#### 5.1.3.2 UART

**Table 5-15 UART pins**

| Pin name | Type | Description |
|---|---|---|
| UART1_RXD | I | Receive data |
| UART1_TXD | O | Transmit data |
| UART2_RXD | I | Receive data |
| UART2_TXD | O | Transmit data |

#### 5.1.3.3 QSPI

**Table 5-16 QSPI pins**

| Pin name | Type | Description |
|---|---|---|
| SPI1_CLK | O | Output clock |
| SPI1_IO[3:0] | IO | I/O data |
| SPI1_SS_N[1:0] | O | Slave select |

#### 5.1.3.4 $I^2C$/SMBus

**Table 5-17 $I^2C$/SMBus pins**

| Pin name | Type | Description |
|---|---|---|
| SMB2_ALERT | IO | $I^2C$/SMBus alert |
| SMB2_CLK | IO | $I^2C$/SMBus clock |
| SMB2_DATA | IO | $I^2C$/SMBus data |
| SMB2_SUSIN | I | $I^2C$/SMBus suspend in |
| SMB2_SUSOUT | O | $I^2C$/SMBus suspend out |
| SMB3_ALERT | IO | $I^2C$/SMBus alert |
| SMB3_CLK | IO | $I^2C$/SMBus clock |
| SMB3_DATA | IO | $I^2C$/SMBus data |
| SMB3_SUSIN | I | $I^2C$/SMBus suspend in |
| SMB3_SUSOUT | O | $I^2C$/SMBus suspend out |
| SMB4_ALERT | IO | $I^2C$/SMBus alert |
| SMB4_CLK | IO | $I^2C$/SMBus clock |
| SMB4_DATA | IO | $I^2C$/SMBus data |
| SMB4_SUSIN | I | $I^2C$/SMBus suspend in |

| Pin name | Type | Description |
|---|---|---|
| SMB4_SUSOUT | O | $I^2C$/SMBus suspend out |

#### *5.1.3.5 GPIOx16/eSPI*

**Table 5-18 GPIOx16/eSPI pins**

| Pin name | Type | Description |
|---|---|---|
| GPIO16_D0_ESPI_IO0 | IO | GPIO data or eSPI data |
| GPIO16_D1_ESPI_IO1 | IO | GPIO data or eSPI data |
| GPIO16_D10_ESPI_ALERT1_N | IO | GPIO data or eSPI alert |
| GPIO16_D11_ESPI_ALERT2_N | IO | GPIO data or eSPI alert |
| GPIO16_D12_ESPI_ALERT3_N | IO | GPIO data or eSPI alert |
| GPIO16_D13_ESPI_RESET_N | IO | GPIO data or eSPI reset |
| GPIO16_D14 | IO | GPIO data or drive 0 |
| GPIO16_D15 | IO | GPIO data or drive 0 |
| GPIO16_D2_ESPI_IO2 | IO | GPIO data or eSPI data |
| GPIO16_D3_ESPI_IO3 | IO | GPIO data or eSPI data |
| GPIO16_D4_ESPI_SS0_N | IO | GPIO data or eSPI slave select |
| GPIO16_D5_ESPI_SS1_N | IO | GPIO data or eSPI slave select |
| GPIO16_D6_ESPI_SS2_N | IO | GPIO data or eSPI slave select |
| GPIO16_D7_ESPI_SS3_N | IO | GPIO data or eSPI slave select |
| GPIO16_D8_ESPI_CLK | IO | GPIO data or eSPI clock |
| GPIO16_D9_ESPI_ALERT0_N | IO | GPIO data or eSPI alert |

#### *5.1.3.6 GPIOx8/QSPI*

**Table 5-19 GPIOx8/QSPI pins**

| Pin name | Type | Description |
|---|---|---|
| GPIO8_C0_SPI2_IO0 | IO | GPIO data or QSPI data |
| GPIO8_C1_SPI2_IO1 | IO | GPIO data or QSPI data |
| GPIO8_C2_SPI2_IO2 | IO | GPIO data or QSPI data |
| GPIO8_C3_SPI2_IO3 | IO | GPIO data or QSPI data |
| GPIO8_C4_SPI2_CLK | IO | GPIO data or QSPI clock |
| GPIO8_C5_SPI2_SS0_N | IO | GPIO data or QSPI slave select |
| GPIO8_C6_SPI2_SS1_N | IO | GPIO data or QSPI slave select |
| GPIO8_C7 | IO | GPIO data or drive 0 |

#### 5.1.3.7 GPIOx8 or I²C/SMBus + I²C/SMBus + UART

**Table 5-20 GPIOx8 or I²C/SMBus + I²C/SMBus + UART pins**

| Pin name | Type | Description |
|---|---|---|
| GPIO8_B0_UART3_RXD | IO | GPIO data or UART data in |
| GPIO8_B1_UART3_TXD | IO | GPIO data or UART data out |
| GPIO8_B2_SMB5_CLK | IO | GPIO data or I²C/SMBus clock |
| GPIO8_B3_SMB5_DATA | IO | GPIO data or I²C/SMBus data |
| GPIO8_B4_SMB6_CLK | IO | GPIO data or I²C/SMBus clock |
| GPIO8_B5_SMB6_DATA | IO | GPIO data or I²C/SMBus data |
| GPIO8_B6 | IO | GPIO data or drive 0 |
| GPIO8_B7 | IO | GPIO data or drive 0 |

### 5.1.4 System Control

**Table 5-21 System control pins**

| Pin name | Type | Description |
|---|---|---|
| BOOT_MODE | I | Boot mode select |
| CMN_TEST_CLK | O | CMN divided by 64 clock |
| GPIO8_A0 | IO | SCP GPIO data |
| GPIO8_A1 | IO | SCP GPIO data |
| GPIO8_A2 | IO | SCP GPIO data |
| GPIO8_A3 | IO | SCP GPIO data |
| GPIO8_A4 | IO | SCP GPIO data |
| GPIO8_A5 | IO | SCP GPIO data |
| GPIO8_A6 | IO | SCP GPIO data |
| GPIO8_A7 | IO | SCP GPIO data |
| REFCLK | I | PLL reference clock (25 or 100 MHz)<br>For details, refer to Reference Clock |
| REFCLK_SEL | I | Reference clock selection:<br>• 0: 25 MHz<br>• 1: 100 MHz<br>**NOTE:** The signal level must correspond to PLL reference clock value. |
| RESET_N | I | Power on reset |
| SMB0_ALERT | IO | SCP SMBus alert |
| SMB0_CLK | IO | SCP SMBus clock |
| SMB0_DATA | IO | SCP SMBus data |
| SMB0_SUSIN | I | SCP SMBus suspend in |
| SMB0_SUSOUT | O | SCP SMBus suspend out |

| Pin name | Type | Description |
|---|---|---|
| SMB1_ALERT | IO | SCP SMBus alert |
| SMB1_CLK | IO | SCP SMBus clock |
| SMB1_DATA | IO | SCP SMBus data |
| SMB1_SUSIN | I | SCP SMBus suspend in |
| SMB1_SUSOUT | O | SCP SMBus suspend out |
| SPI0_CLK | O | SCP SPI clock |
| SPI0_RXD | I | SCP SPI data in |
| SPI0_SS_N[1:0] | O | SCP SPI slave select |
| SPI0_TRAIN_OFF | I | SPI training off |
| SPI0_TXD | O | SCP SPI data out |
| UART0_RXD | I | SCP UART receive data |
| UART0_TXD | O | SCP UART transmit data |
| WDT_RESET | O | WDT reset |

### 5.1.5 System Debug

**Table 5-22 System debug pins**

| Pin name | Type | Description |
|---|---|---|
| CS_TCK | I | CoreSight input clock |
| CS_TDI | I | CoreSight data in |
| CS_TDO | O | CoreSight data out |
| CS_TMS | I | CoreSight test mode |
| CS_TRST_N | I | CoreSight reset |

### 5.1.6 Power and Ground

#### 5.1.6.1 Core Supply

**Table 5-23 Core supply pins**

| Pin name | Type | Description |
|---|---|---|
| VDD | P | Core power (0.9 V default) |

#### 5.1.6.2 0.85V Voltage Supply

**Table 5-24 0.85V voltage supply pins**

| Pin name | Type | Description |
|---|---|---|
| VDD_PCIE0_VP | P | PCIe analog voltage supply (0.85 V) |
| VDD_PCIE1_VP | P | PCIe analog voltage supply (0.85 V) |
| VDD_PCIE2_VP | P | PCIe analog voltage supply (0.85 V) |
| VDD_PCIE3_VP | P | PCIe analog voltage supply (0.85 V) |

| Pin name | Type | Description |
|---|---|---|
| VDD_PCIE4_VP | P | PCIe analog voltage supply (0.85 V) |

#### *5.1.6.3 PLL Supply*

**Table 5-25 PLL supply pins**

| Pin name | Type | Description |
|---|---|---|
| VDD_PLL | P | PLL analog voltage supply (1.8 V) |

#### *5.1.6.4 DDR Supply*

**Table 5-26 DDR supply pins**

| Pin name | Type | Description |
|---|---|---|
| VDDQ012 | P | DDR VDDQ voltage supply (1.2 V for DDR4) |
| VDDQ345 | P | DDR VDDQ voltage supply (1.2 V for DDR4) |

#### *5.1.6.5 DDR PLL Supply*

**Table 5-27 DDR PLL supply pins**

| Pin name | Type | Description |
|---|---|---|
| VDD_DDR_PLL | P | DDR PLL voltage supply (1.8 V default) |

#### *5.1.6.6 1.8V Voltage Supply*

**Table 5-28 1.8V voltage supply pins**

| Pin name | Type | Description |
|---|---|---|
| VDD_PCIE0_VPH | P | PCIe I/O Voltage supply (1.8 V default) |
| VDD_PCIE1_VPH | P | PCIe I/O Voltage supply (1.8 V default) |
| VDD_PCIE2_VPH | P | PCIe I/O Voltage supply (1.8 V default) |
| VDD_PCIE3_VPH | P | PCIe I/O Voltage supply (1.8 V default) |
| VDD_PCIE4_VPH | P | PCIe I/O Voltage supply (1.8 V default) |
| VDD_PVT | P | PVT analog voltage supply (1.8 V) |
| VDDIO | P | IO voltage supply (1.8 V) |

#### *5.1.6.7 Ground*

**Table 5-29 Ground pins**

| Pin name | Type | Description |
|---|---|---|
| VSS | G | Core ground supply |
| VSSIO | G | IO ground supply |

### *5.1.7 Requirements for Unused Pins*

The following table shows the requirements for unused pins of the BE-S1000. Please follow these requirements if you are not going to use any interface from **Pinout List**.

**Table 5-30 Requirements for unused pins**

| Type | Requirements |
|---|---|
| Input pins | Tie to ground potential<br>If active level is low, tie to power supply |
| Output pins | Leave floating |
| Power pins | Always use |
| Reserved pins | Leave floating |

## 5.2 Pin Map Overview

The following diagram shows ball map from the top view of the package.

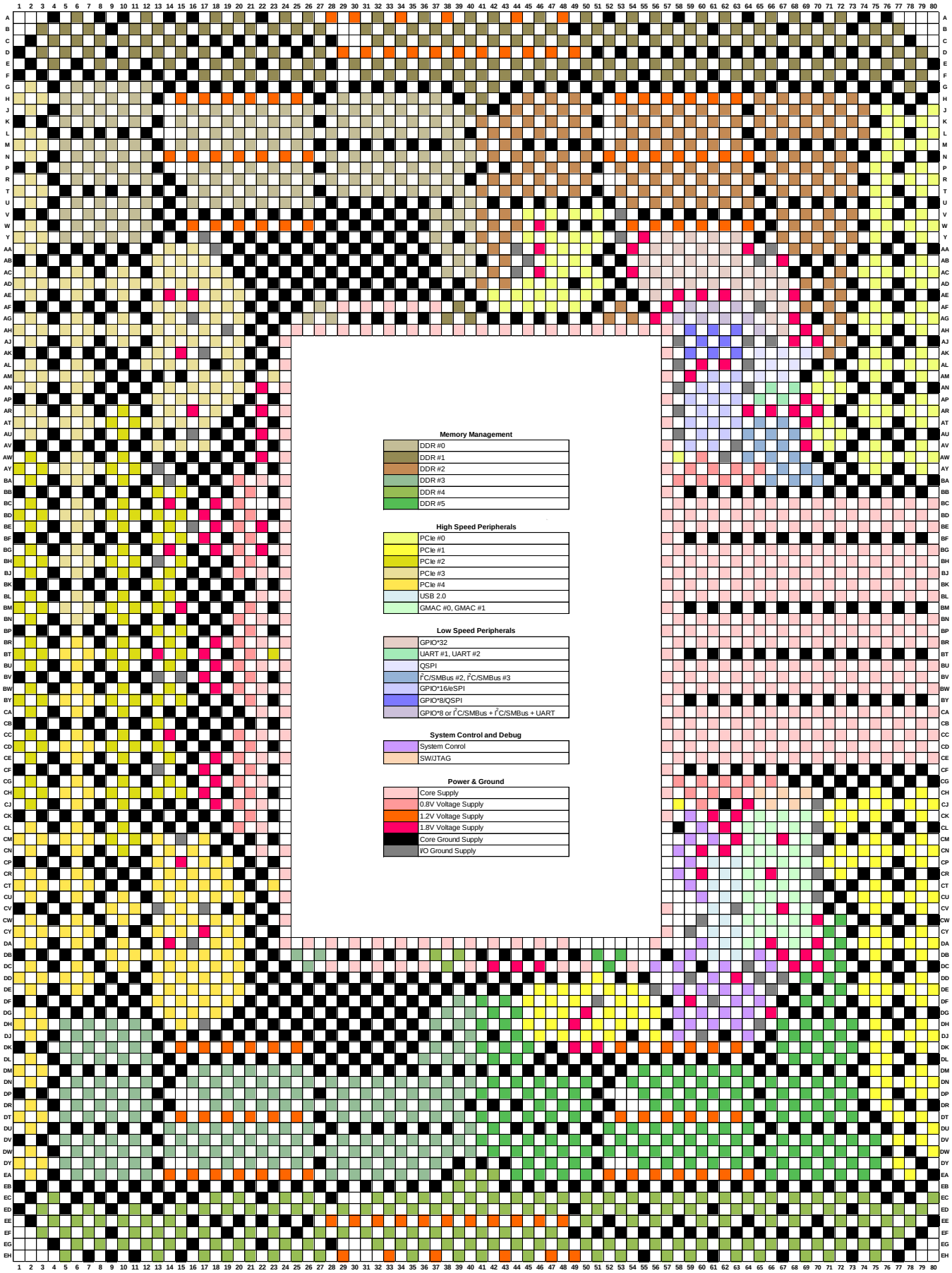



**Figure 5-1 BE-S1000 pin map**

### 5.2.1 Power and Ground

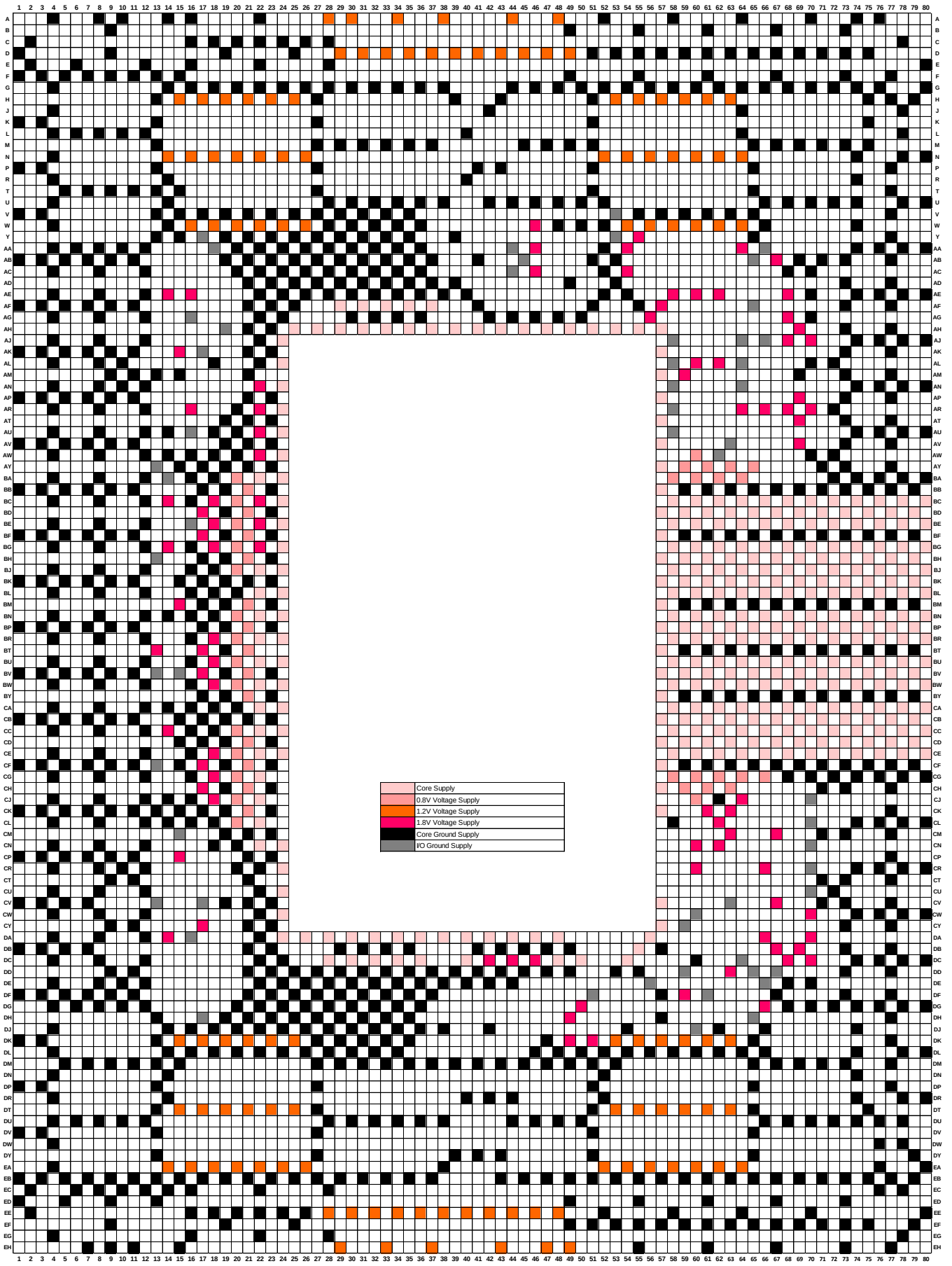



**Figure 5-2 Power and ground pin placement**

### 5.2.2 High Speed Peripherals

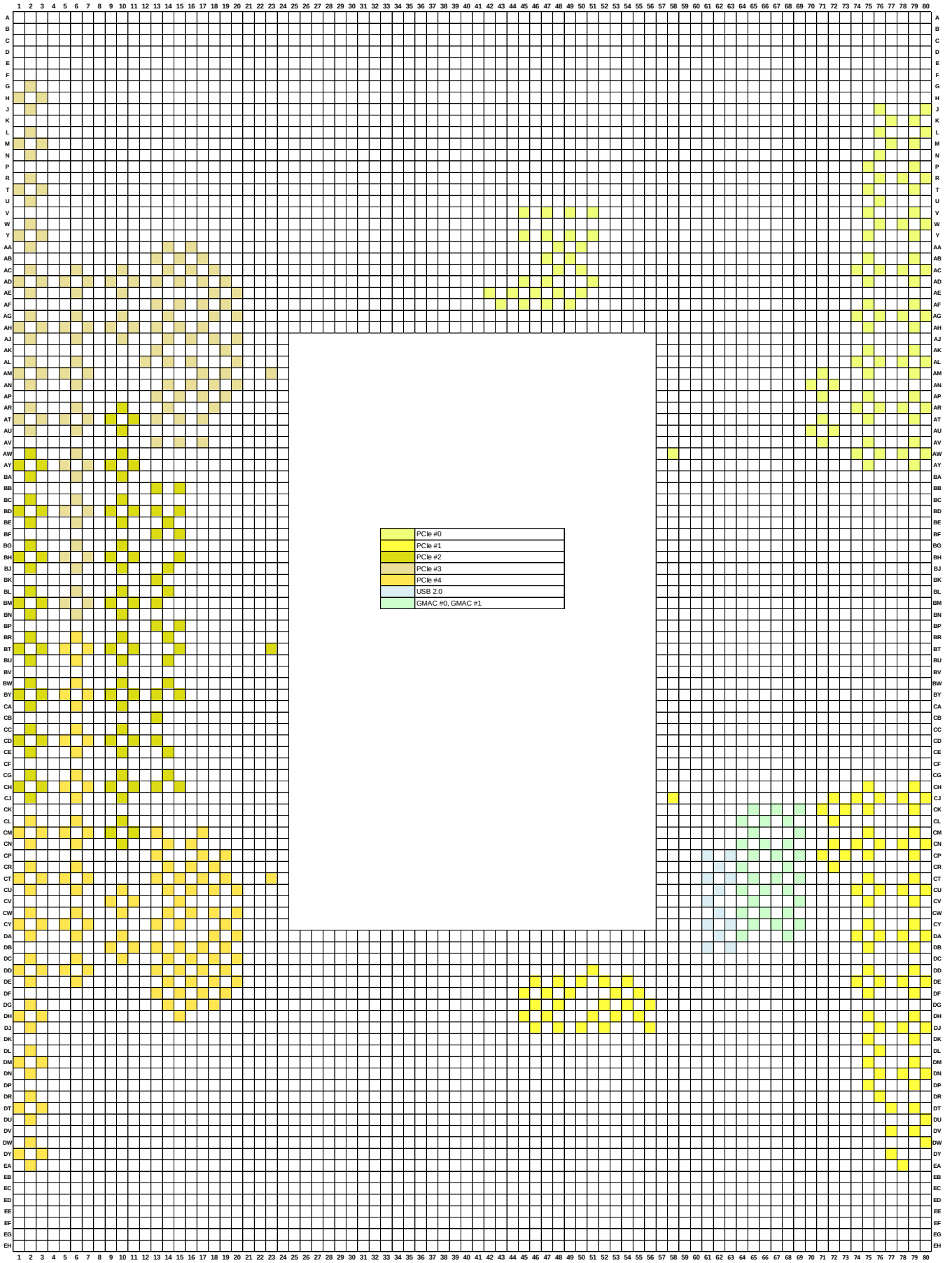



**Figure 5-3 High speed peripherals pin placement**

### 5.2.3 Low Speed Peripherals

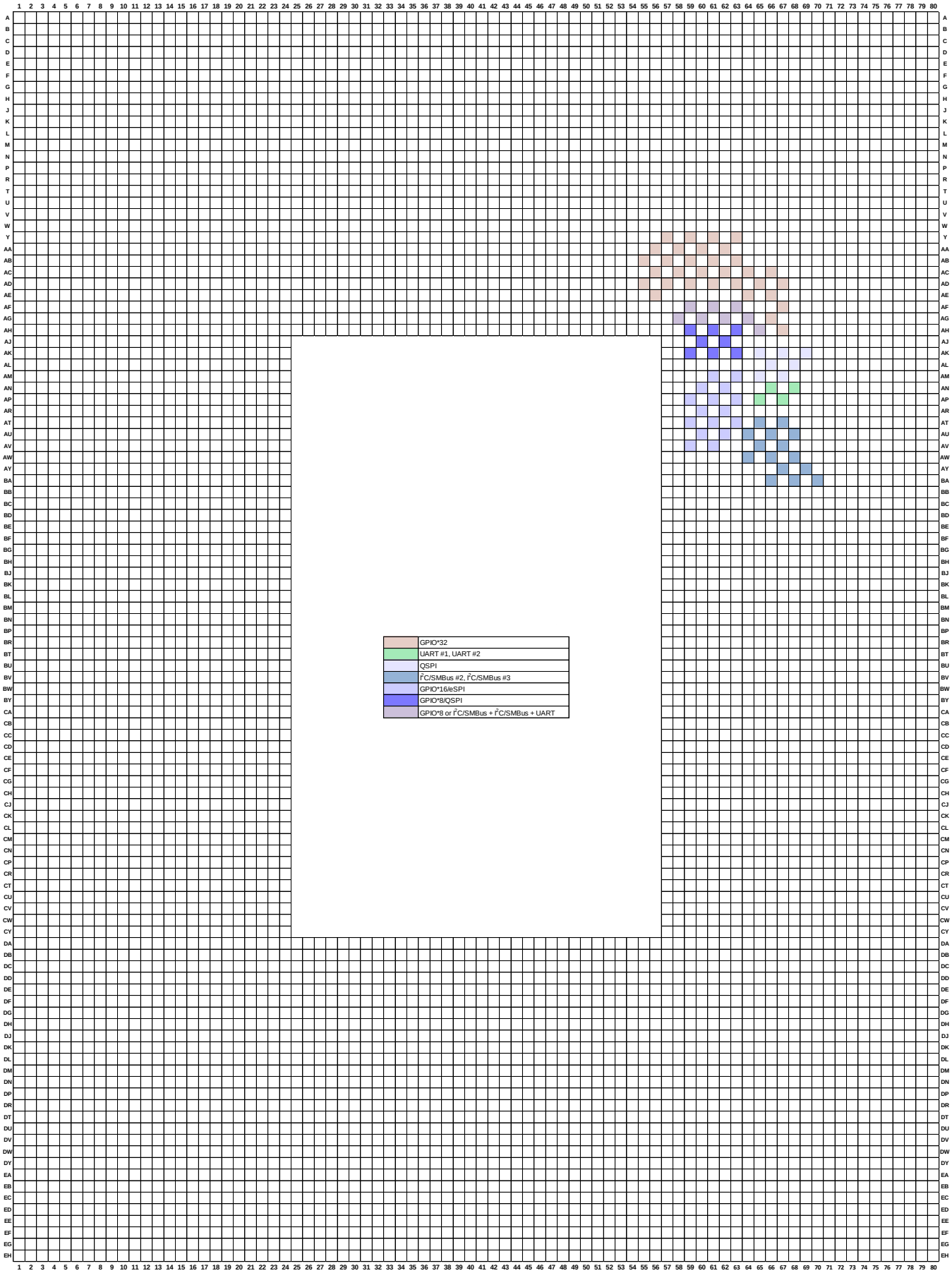



**Figure 5-4 Low speed peripherals pin placement**

### 5.2.4 Memory

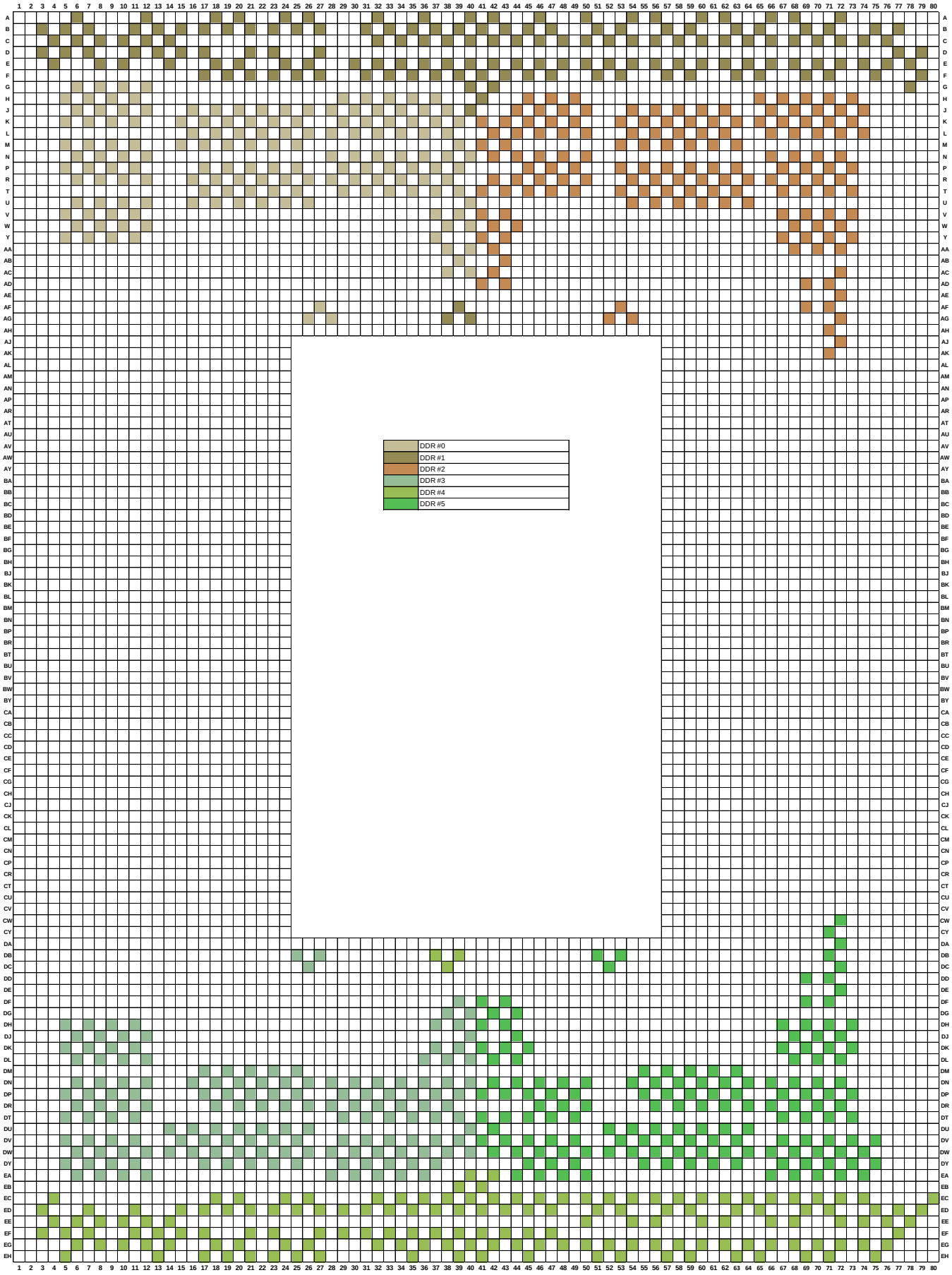



**Figure 5-5 Memory pin placement**

### 5.2.5 System Control and Debug

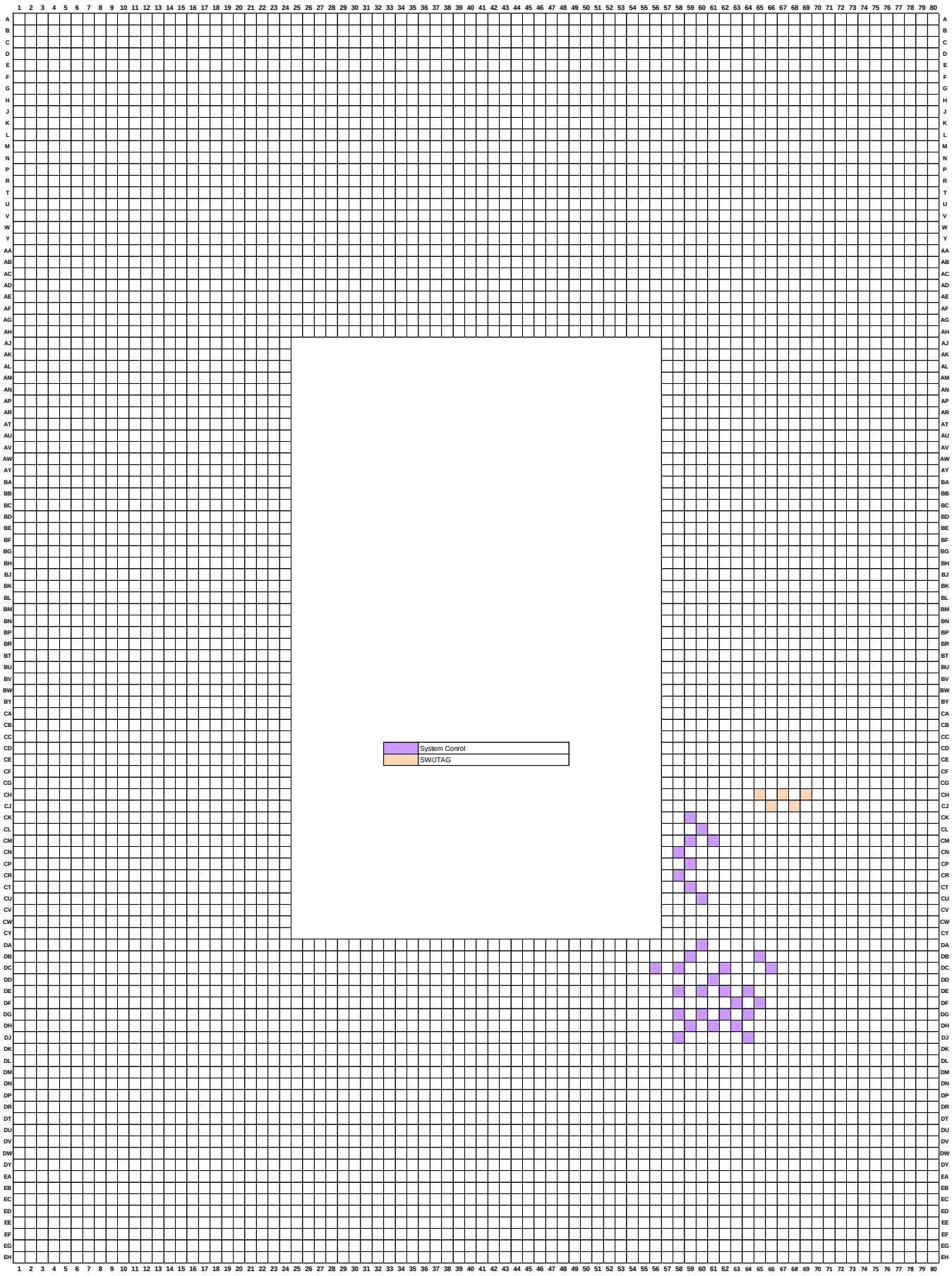



**Figure 5-6 System control and debug pin placement**

### 5.2.6 Detailed Pin Map

The following figure shows the division of BE-S1000 pin map into twelve sections (A, B, C, D, E, F, G, H, I and J).

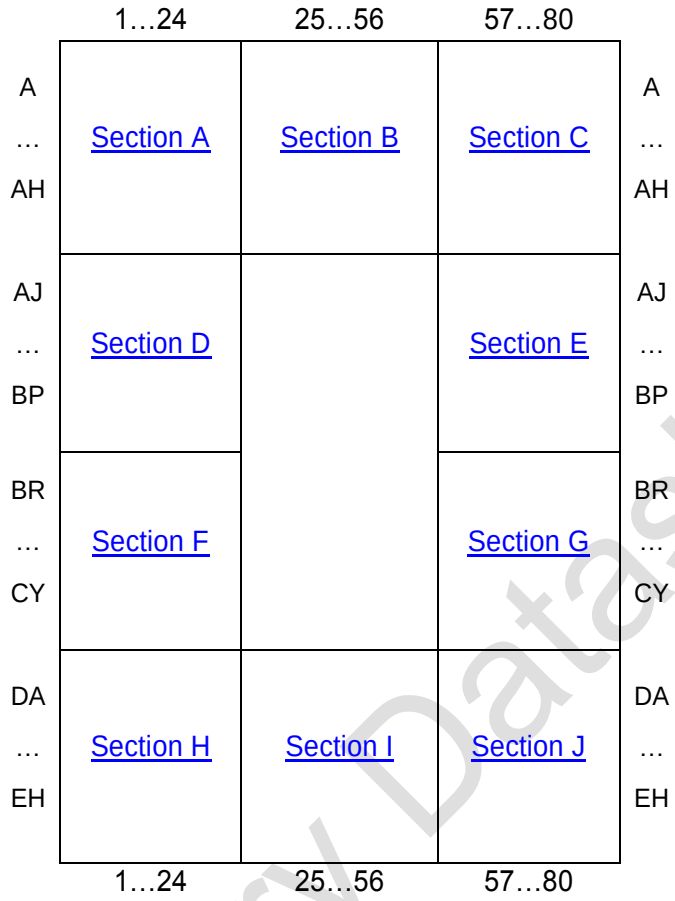



**Figure 5-7 BE-S1000 pin map division**

### 5.2.6.1 Section A

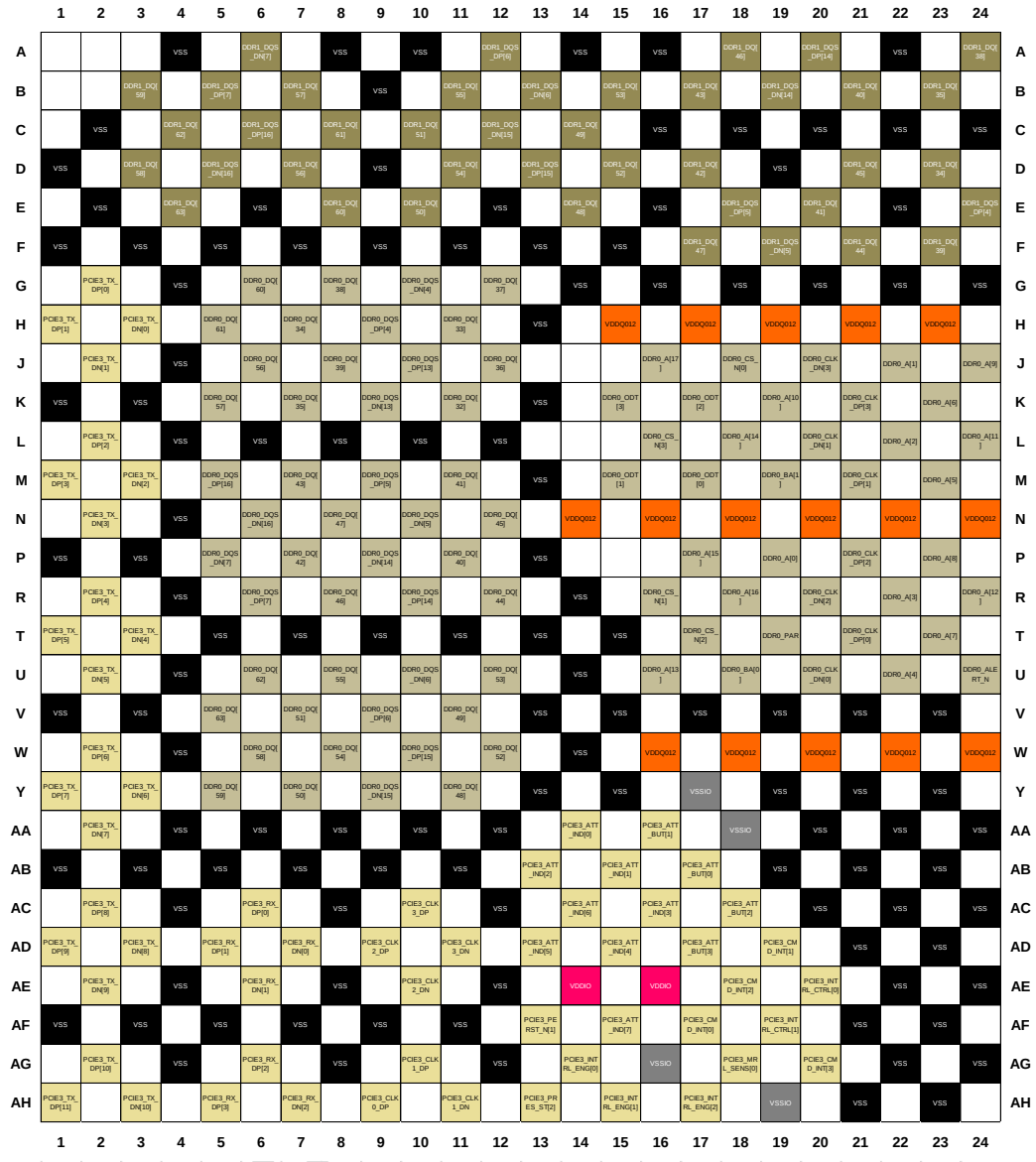



**Figure 5-8 BE-S1000 pin map (section A)**

### 5.2.6.2 Section B

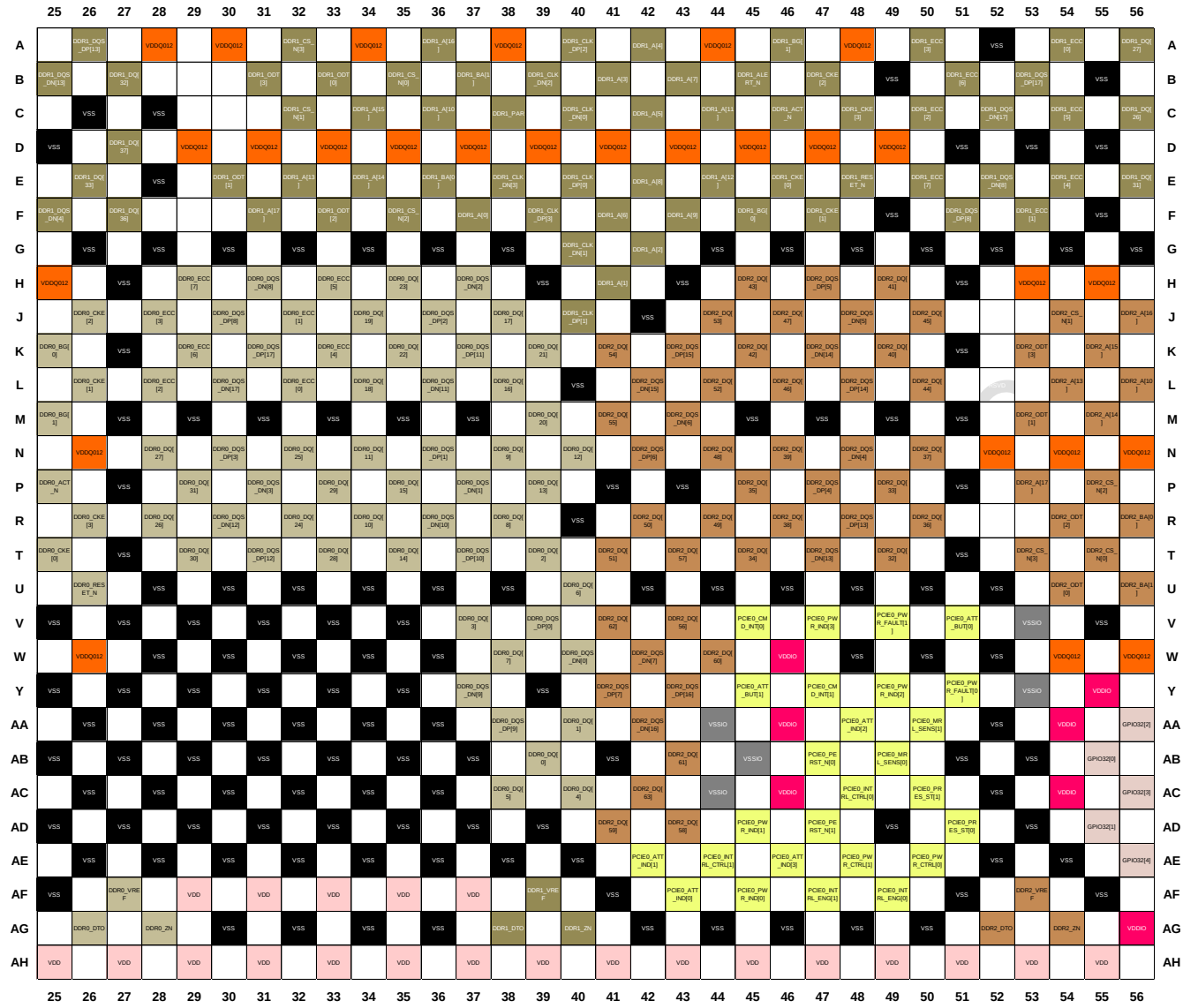



**Figure 5-9 BE-S1000 pin map (section B)**

### 5.2.6.3 Section C

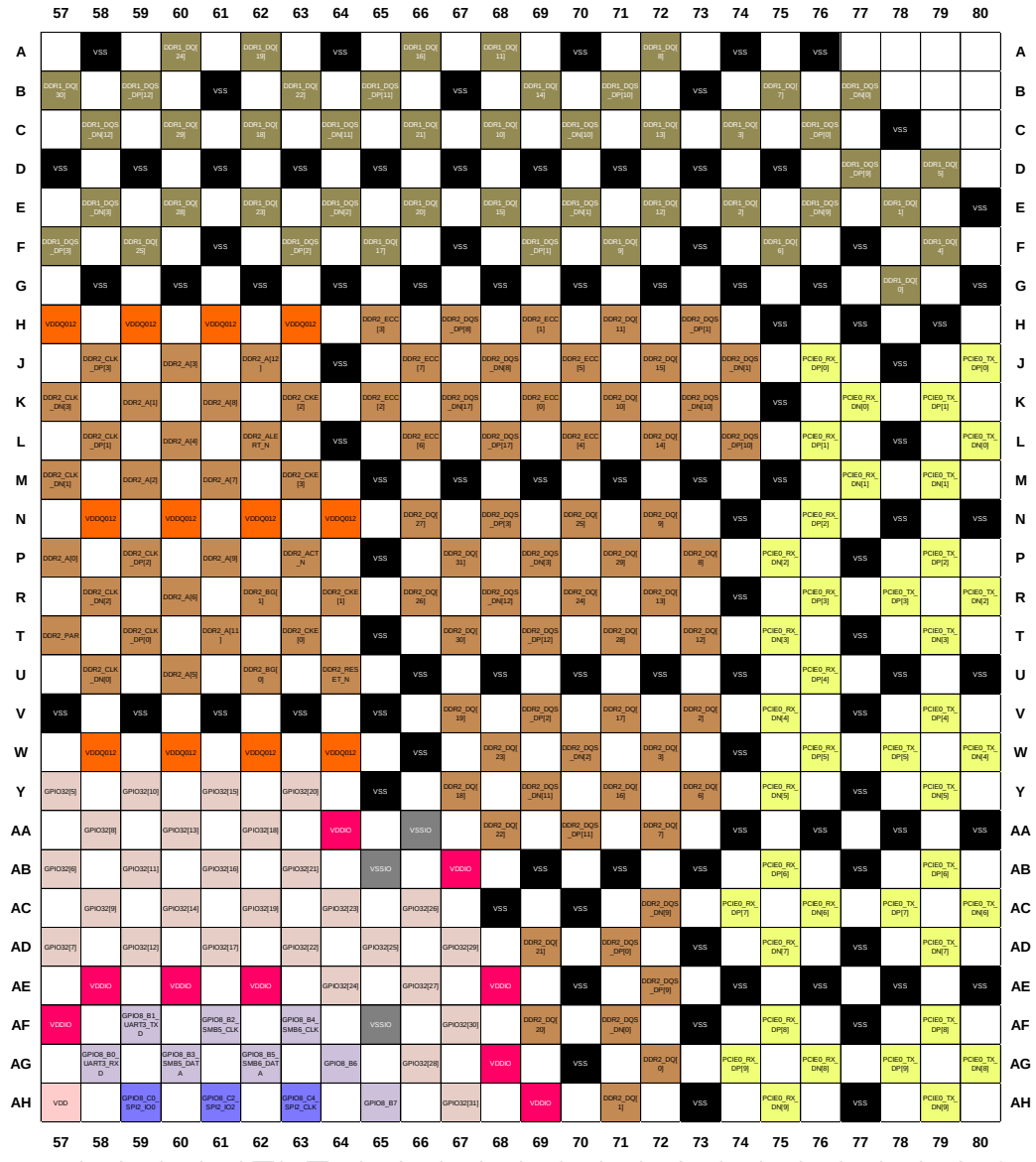



**Figure 5-10 BE-S1000 pin map (section C)**

### 5.2.6.4 Section D

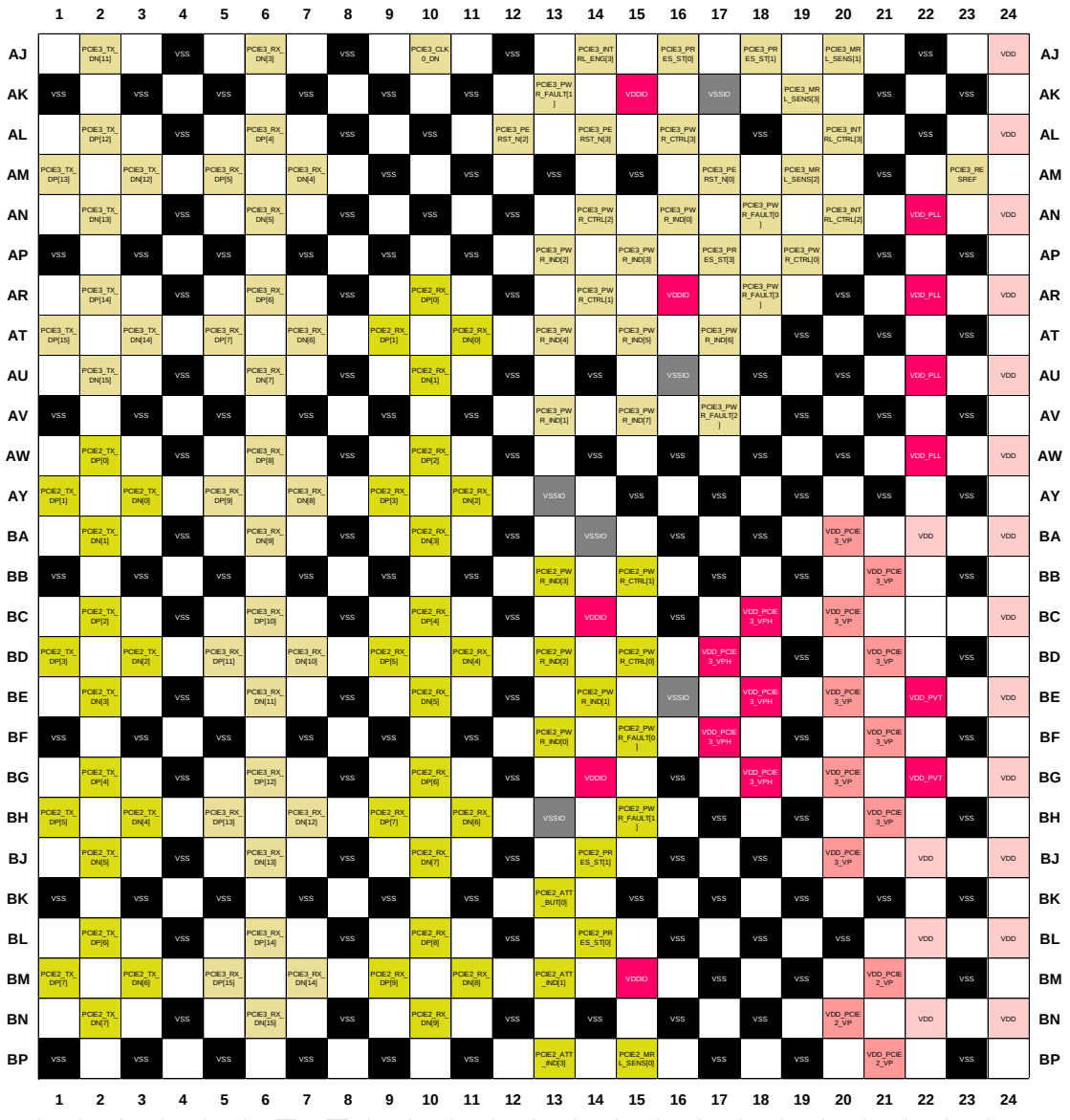



**Figure 5-11 BE-S1000 pin map (section D)**

### 5.2.6.5 Section E

| | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AJ | | VSSIO | | GPIO8_C1_SPI2_IO1 | | GPIO8_C3_SPI2_IO3 | | VSSIO | | VSSIO | | VDDIO | | VDDIO | | DDR2_DQ[4] | | VSS | | VSS | | VSS | | VSS | AJ |
| AK | VDD | | GPIO8_C5_SPI2_SS0_N | | GPIO8_C6_SPI2_SS1_N | | GPIO8_C7 | | SPI1_CLK | | SPI1_IO[1] | | SPI1_IO[3] | | DDR2_DQ[5] | | VSS | | PCIE0_RX_DP[10] | | VSS | | PCIE0_TX_DP[10] | | AK |
| AL | | VSSIO | | VDDIO | | VDDIO | | VSSIO | | SPI1_IO[0] | | SPI1_IO[2] | | VSS | | VSS | | PCIE0_RX_DP[11] | | PCIE0_RX_DN[10] | | PCIE0_TX_DP[11] | | PCIE0_TX_DN[10] | AL |
| AM | VDD | | VDDIO | | GPIO16_D1_ESPI_IO1 | | GPIO16_D3_ESPI_IO3 | | SPI1_SS_N[0] | | SPI1_SS_N[1] | | VSS | | PCIE0_CLK3_DP | | VSS | | PCIE0_RX_DN[11] | | VSS | | PCIE0_TX_DN[11] | | AM |
| AN | | VSSIO | | GPIO16_D0_ESPI_IO0 | | GPIO16_D2_ESPI_IO2 | | VSSIO | | UART1_RXD | | UART1_TXD | | PCIE0_CLK2_DP | | PCIE0_CLK3_DN | | VSS | | VSS | | VSS | | VSS | AN |
| AP | VDD | | GPIO16_D6_ESPI_SS2_N | | GPIO16_D5_ESPI_SS1_N | | GPIO16_D4_ESPI_SS0_N | | UART2_RXD | | UART2_TXD | | VDD_PCIE0_VPH | | PCIE0_CLK2_DN | | VSS | | PCIE0_RX_DP[12] | | VSS | | PCIE0_TX_DP[12] | | AP |
| AR | | VSSIO | | GPIO16_D7_ESPI_SS3_N | | GPIO16_D8_ESPI_CLK | | VDDIO | | VDDIO | | VDD_PCIE0_VPH | | VDD_PCIE0_VPH | | VSS | | PCIE0_RX_DP[13] | | PCIE0_RX_DN[12] | | PCIE0_TX_DP[13] | | PCIE0_TX_DN[12] | AR |
| AT | VDD | | GPIO16_D11_ESPI_ALERT2_N | | GPIO16_D10_ESPI_ALERT1_N | | GPIO16_D9_ESPI_ALERT0_N | | SMB2_CLK | | SMB2_SUSIN | | VDD_PCIE0_VPH | | PCIE0_CLK1_DP | | VSS | | PCIE0_RX_DN[13] | | VSS | | PCIE0_TX_DN[13] | | AT |
| AU | | VSSIO | | GPIO16_D12_ESPI_ALERT3_N | | GPIO16_D13_ESPI_RESET_N | | SMB2_DATA | | SMB2_SUSOUT | | SMB2_ALERT | | PCIE0_CLK0_DP | | PCIE0_CLK1_DN | | VSS | | VSS | | VSS | | VSS | AU |
| AV | VDD | | GPIO16_D14 | | GPIO16_D15 | | VSSIO | | SMB3_CLK | | SMB3_SUSIN | | VDD_PCIE0_VPH | | PCIE0_CLK0_DN | | VSS | | PCIE0_RX_DP[14] | | VSS | | PCIE0_TX_DP[14] | | AV |
| AW | | PCIE0_RESREF | | VDD_PCIE0_VP | | VSSIO | | SMB3_DATA | | SMB3_SUSOUT | | SMB3_ALERT | | VSS | | VSS | | PCIE0_RX_DP[15] | | PCIE0_RX_DN[14] | | PCIE0_TX_DP[15] | | PCIE0_TX_DN[14] | AW |
| AY | VDD | | VDD_PCIE0_VP | | VDD_PCIE0_VP | | VDD_PCIE0_VP | | VDD_PCIE0_VP | | SMB4_CLK | | SMB4_SUSIN | | VSS | | VSS | | PCIE0_RX_DN[15] | | VSS | | PCIE0_TX_DN[15] | | AY |
| BA | | VDD_PCIE0_VP | | VDD_PCIE0_VP | | VDD_PCIE0_VP | | VDD_PCIE0_VP | | SMB4_DATA | | SMB4_SUSOUT | | SMB4_ALERT | | VSS | | VSS | | VSS | | VSS | | VSS | BA |
| BB | VDD | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | BB |
| BC | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | BC |
| BD | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | BD |
| BE | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | BE |
| BF | VDD | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | BF |
| BG | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | BG |
| BH | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | BH |
| BJ | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | BJ |
| BK | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | BK |
| BL | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | BL |
| BM | VDD | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | VSS | | BM |
| BN | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | BN |
| BP | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | VDD | | BP |
| | 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | |

**Figure 5-12 BE-S1000 pin map (section E)**

### 5.2.6.6 Section F

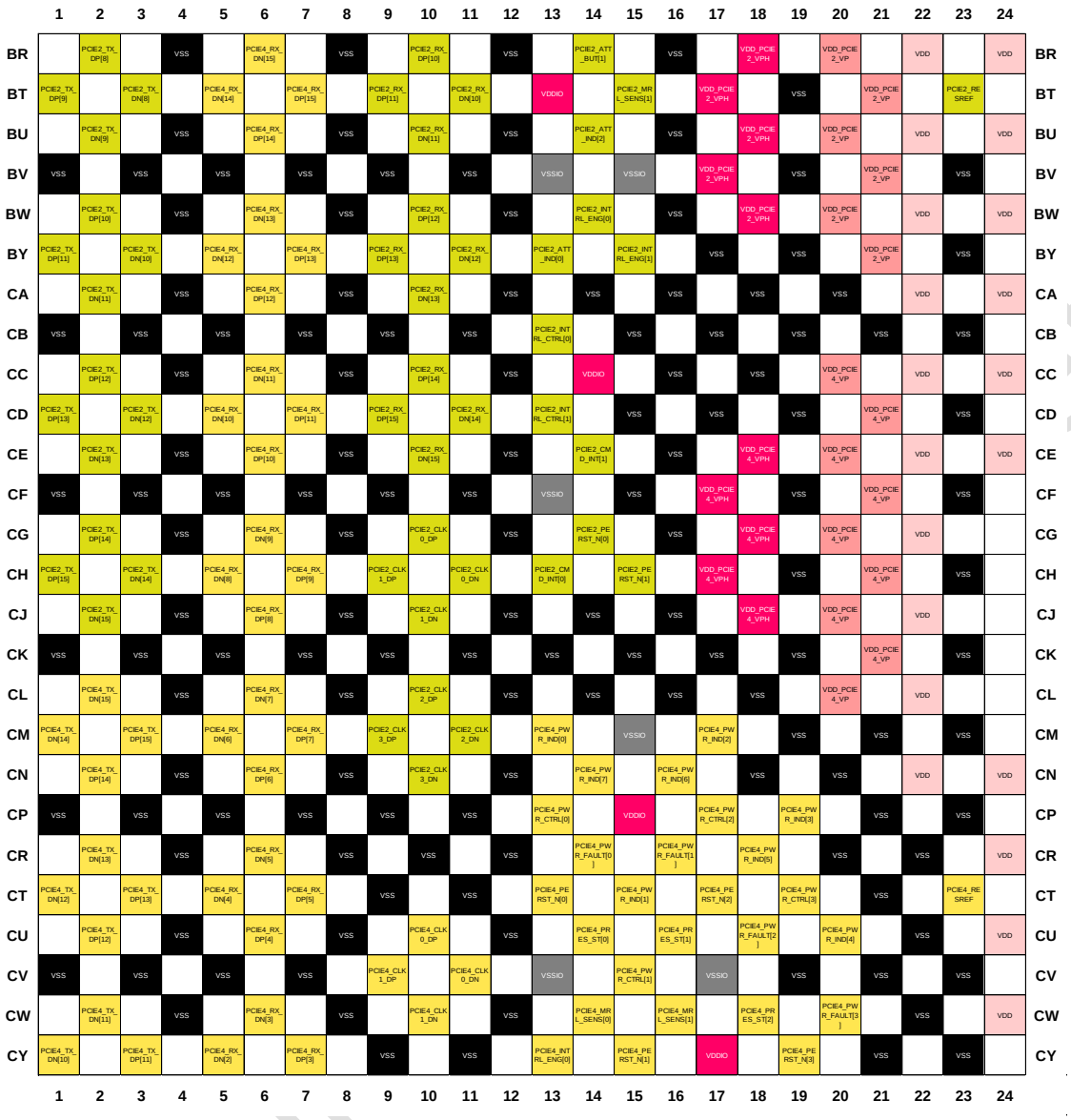



**Figure 5-13 BE-S1000 pin map (section F)**

### 5.2.6.7 Section G

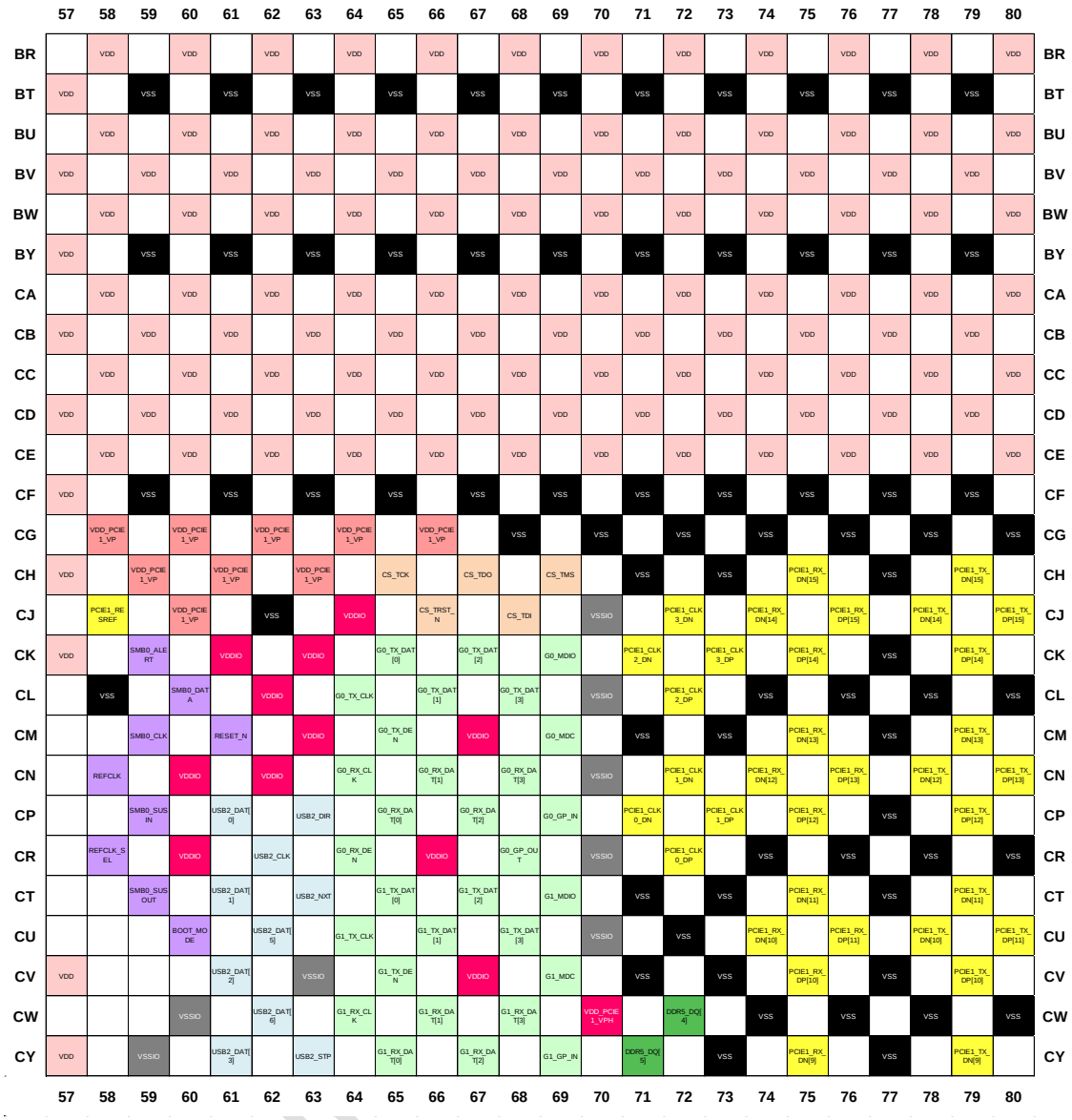



**Figure 5-14 BE-S1000 pin map (section G)**

### 5.2.6.8 Section H

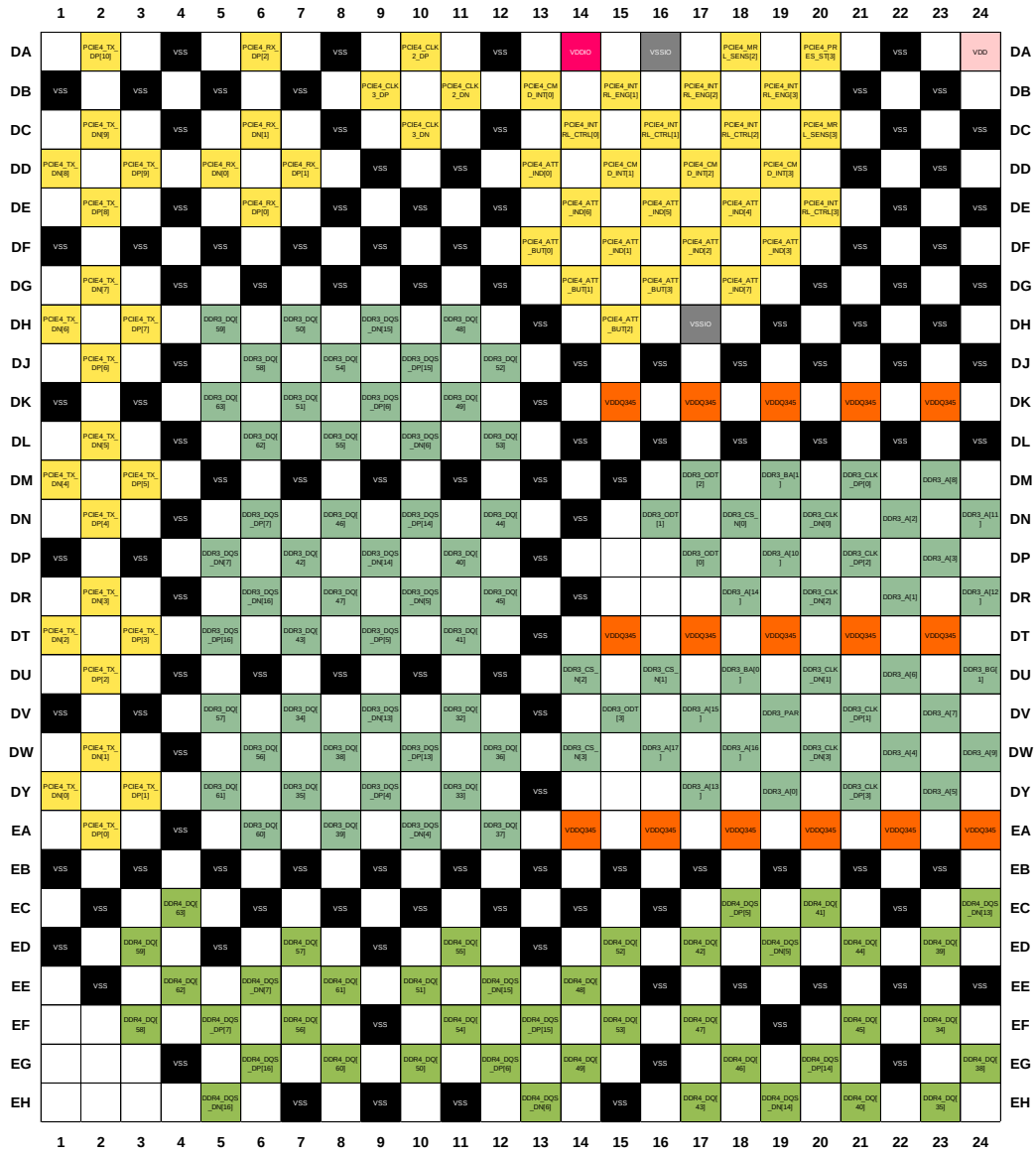


Figure 5-15 BE-S1000 pin map (section H)

### 5.2.6.9 Section I

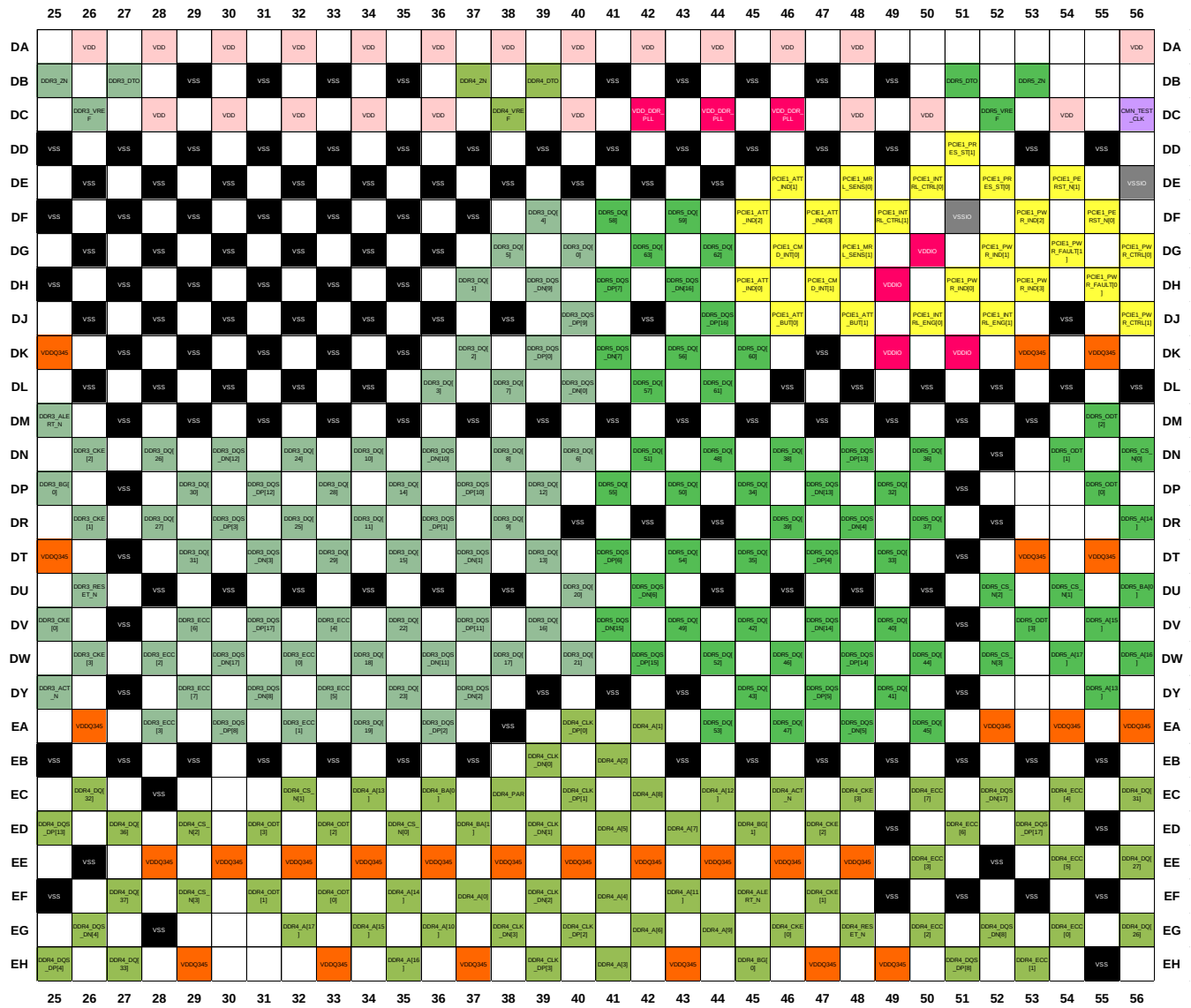



**Figure 5-16 BE-S1000 pin map (section I)**

### 5.2.6.10 Section J

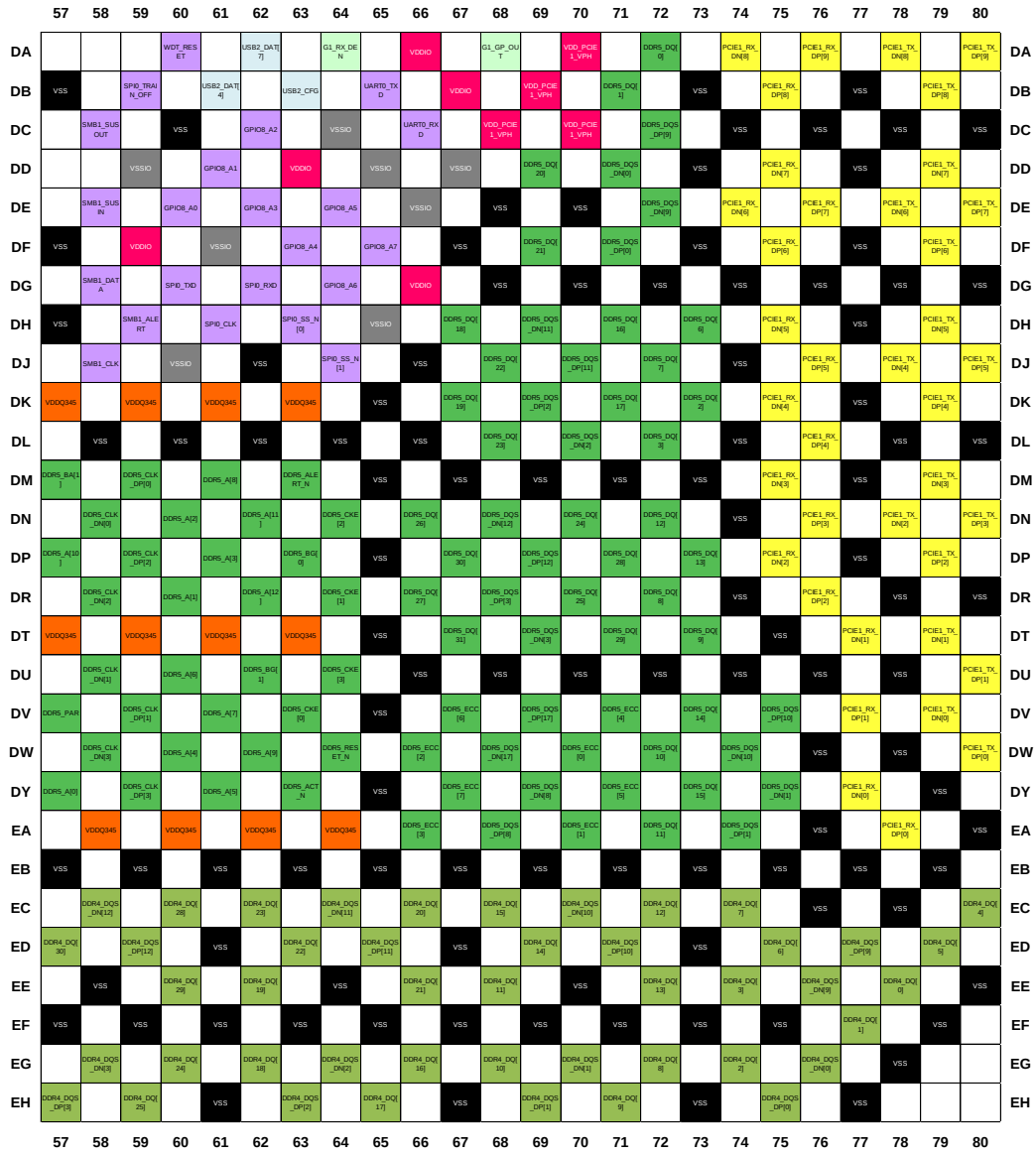



**Figure 5-17 BE-S1000 pin map (section J)**

# 6 Package and Ordering Information

## 6.1 Ordering information

BE-S1000 is an orderable part number. Designation of each field in the part number is shown in a table below.

**Table 6-1 Ordering information**

| BE | - | S | 1 | 0 | 0 | 0 | X |
|---|---|---|---|---|---|---|---|
| Baikal Electronics | Field Delimiter | Product Line | Generation | Modification | Reserved Field | Reserved Field | Corner |

BE-S1000 is the first product in the BE-S product line.

To order BE-S1000, please contact BAIKAL ELECTRONICS company.

## 6.2 Marking

The following table shows designation of each field in the package marking of BE-S1000.

**Table 6-2 BE-S1000 package marking**

| A | K | . | YY | WW |
|---|---|---|---|---|
| Type of a set of photomasks | Manufacturer of the substrate housing | Field Delimiter | Year | Week |

## 6.3 FCLGA-3467 Package

The SoC is mounted into FCLGA-3467 package. Main package parameters are shown in the following figures.

**NOTE:** The package size values are represented in mm.

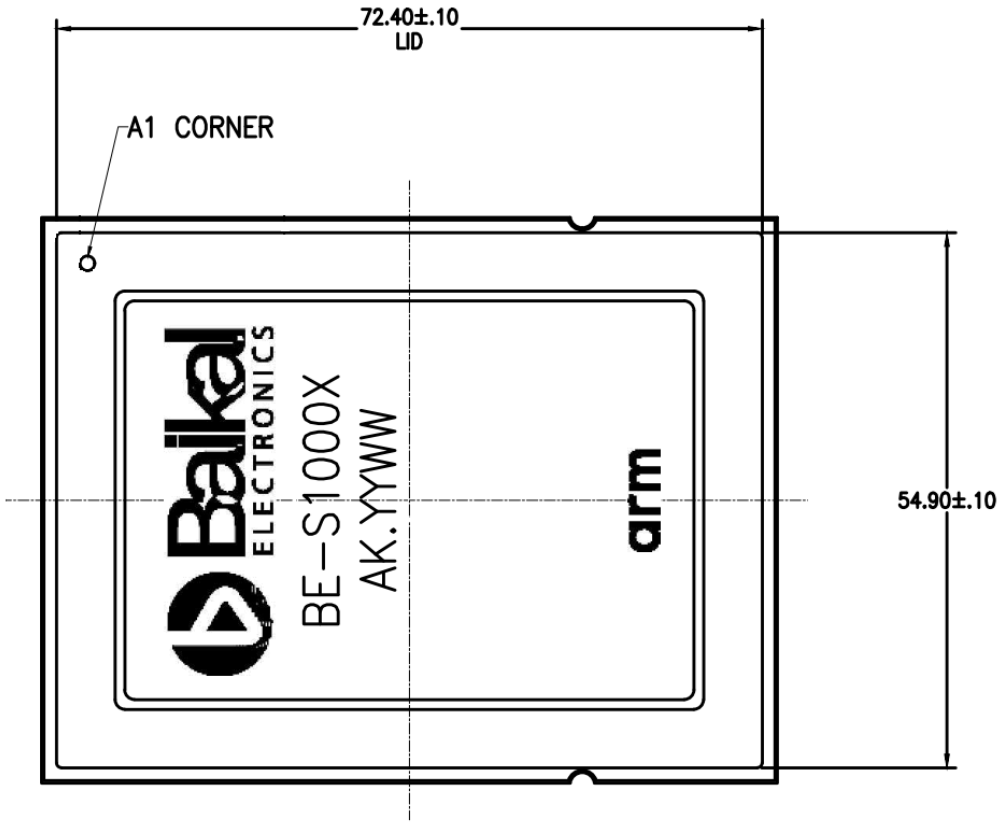



**Figure 6-1 BE-S1000 package. Top view**

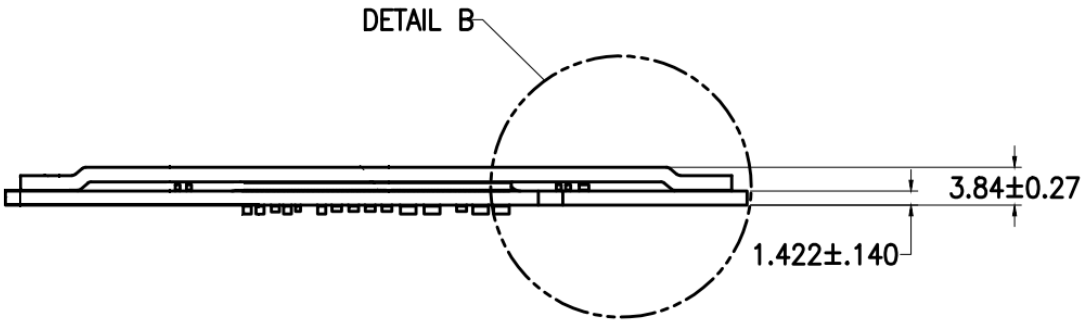



**Figure 6-2 BE-S1000 package. Side view**

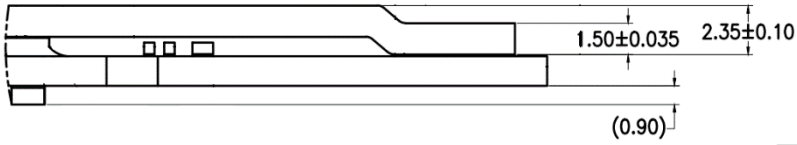



**Figure 6-3 Detail B**

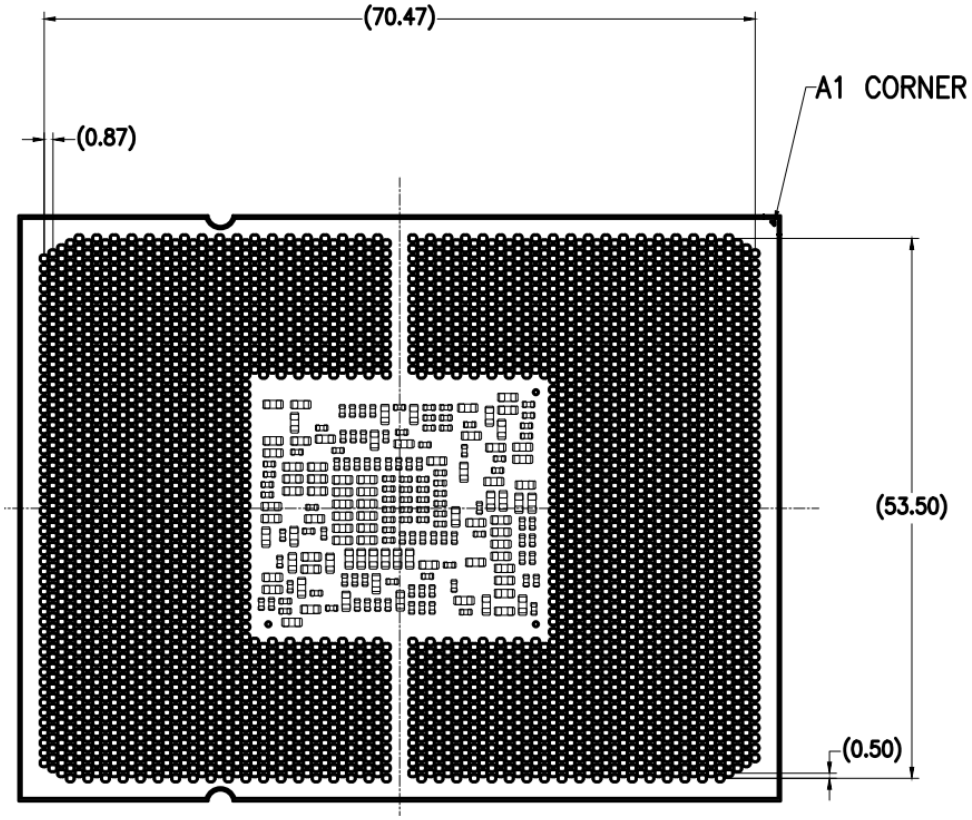



**Figure 6-4 BE-S1000 package. Bottom view**

## 6.4 Delivery Set

The following standart components are included in the delivery set:

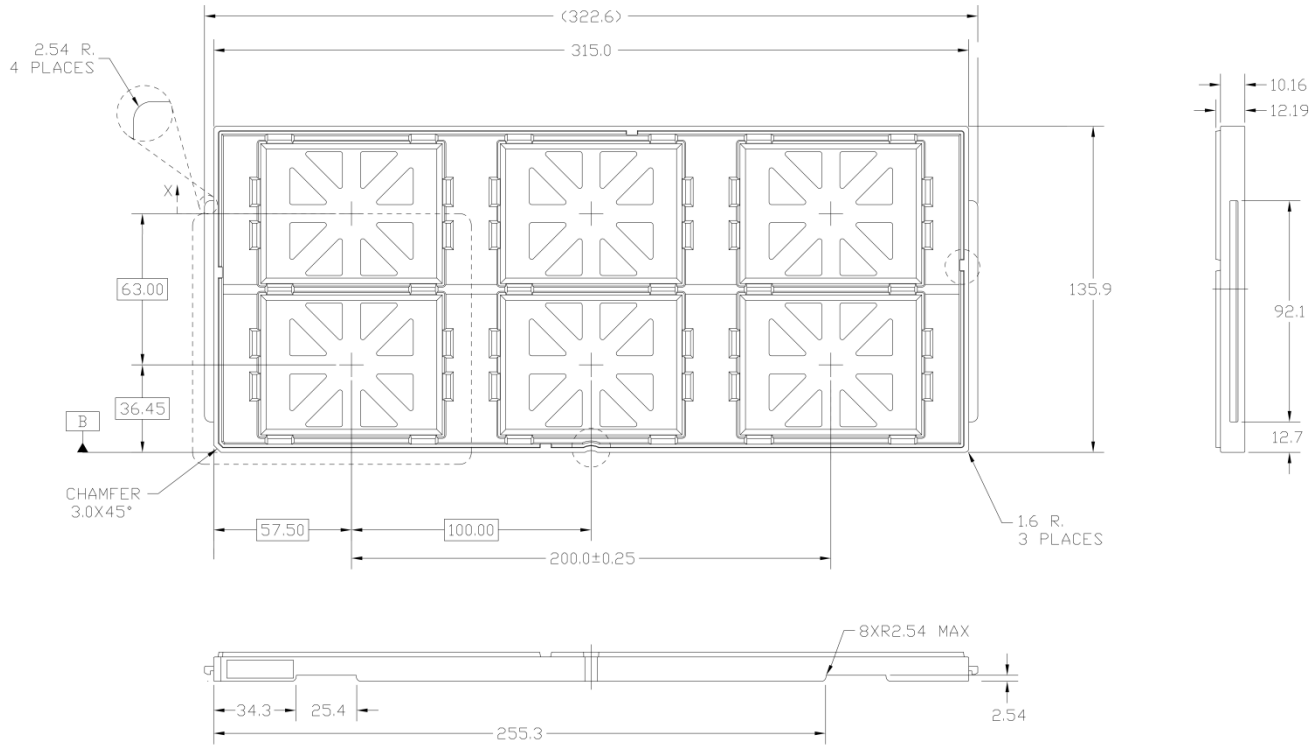
- Socket
- Heatsink

A detailed description of each element and its packaging is given in the document *Microprocessor BE-S1000. Thermo-Mechanical Design Guide* (**TMDG**).

> **ATTENTION:** It's unacceptable to use a microprocessor without a radiator. The manufacturer isn't responsible for the performance of the microprocessor when using a non-standard radiator.

## 6.5 Packing

The microprocessors are supplied in plastic containers (in the amount of 1 to 6 pieces each), as shown in the following figure.




**Fisure 6-5 – BE-S1000 packaging**

Plastic containers are placed in sealed packaging containing moisture absorption and humidity control means (indicator card). The sealed package is placed in a cardboard shipping box. The permissible time of atmospheric exposure may be indicated on sealed plastic packages.

The unused space is filled with a soft sealing material.

The space between trays is padded with a soft sealing material.

# 7 Support

## 7.1 Documentation

The following documents describe the BE-S1000 microprocessor and provide information for board designers and system programmers:

- Power Supply Requirements
- Application Design Guide
- Thermo-Mechanical Design Guide
- Programming Guide

### *7.1.1 Power Supply Requirements*

Each power domain of BE-S1000 requires the use of special filters on the power supply. The power supply requirements are described in the document written in Russia under the title «Микропроцессор BE-S1000 Требования к источникам питания». The power supply requirements are under development and will be available in Russian only.

### *7.1.2 Application Design Guide*

The *Application Design Guide* (**ADG**) describes how to design the BE-S1000 physical interfaces on a board.

ADG is under development and will be available in English only.

To request the guide, please contact BAIKAL ELECTRONICS support. **NDA is required**.

The following table describes the guide content.

**Table 7-1 BE-S1000 application design guide**

| Volume | Title |
|---|---|
| 1 | DDR4 |
| 2 | PCIe |
| 3 | USB 2.0 |
| 4 | 1 Gb Ethernet |
| 5 | eSPI |
| 6 | QSPI |
| 7 | UART |
| 8 | GPIO |
| 9 | JTAG |
| 10 | $I^2C$/SMBus |

### *7.1.3 Thermo-Mechanical Design Guide*

The TMDG is intended to assist board and system thermal mechanical designers, as well as designers and suppliers of processor heatsinks.

TMDG is under development in Russian only (under the title «Руководство по термомеханическому проектированию»).

### *7.1.4 Programming Guide*

The *Programming Guide* (**PG**) describes how to program the microprocessor subsystems and provides information for developers of device drivers or bare-metal applications.

The following table describes the guide content.

**Table 7-2 BE-S1000 programming guide**

| | Volume | Title |
|---|---|---|
| 1 | 1 | General Description |
| 2 | 2 | Memory Map |
| 3 | 3 | Interrupts |
| | **SoC Interconnects** | |
| 4 | 4.1 | Network Interconnect (NIC) |
| 5 | 4.2 | Coherent Mesh Network (CMN) |
| | **System Debug** | |
| 6 | 5 | CoreSight Subsystem |
| | **System Monitoring and Management** | |
| 7 | 6.1 | Local Clock and Reset Unit (LCRU) |
| 8 | 6.2 | Process, Voltage and Temperature (PVT) Sensors |
| | **Memory Management** | |
| 9 | 7.1 | DDR4 Memory Controller |
| 10 | 7.2 | DDR PHY |
| 11 | 7.3 | System Memory Management Unit (SMMU) |
| | **Connectivity & Mass Storage** | |
| 12 | 8.1 | PCIe RootComplex Controller |
| 13 | 8.2 | PCIe Dual Mode (CCIX/RC) Controller |
| 14 | 8.3 | PCIe Subsystem APB Bridge |
| 15 | 8.4 | PCIe PHY |
| 16 | 8.5 | 1Gb Ethernet MAC (GMAC) |
| 17 | 8.6 | USB 2.0 Controller |
| | **Timers** | |
| 18 | 9.1 | Cortex-A75 Timers |
| 19 | 9.2 | Peripheral Timers |
| 20 | 9.3 | Watchdog Timer |
| | **Low Speed Peripherals** | |
| 21 | 10.1 | I2C/System Management Bus Controller (I2C/SMBus) |
| 22 | 10.2 | Quad Serial Peripheral Interface (QSPI) |
| 23 | 10.3 | Enhanced Serial Peripheral Interface (eSPI) |
| 24 | 10.4 | Universal Asynchronous Receiver/Transmitter, Type «A» (UART_A) |
| 25 | 10.5 | Universal Asynchronous Receiver/Transmitter, Type «S» (UART_S) |
| 26 | 10.6 | General Purpose Input/Output (GPIO) |

PG is under development and will be available in English only.

To request the guide, please contact BAIKAL ELECTRONICS support. **NDA is required**.

## 7.2 SDK

BAIKAL ELECTRONICS produces the *Software Development Kit* (**SDK**) ARM64, which provides software support for the BE-S1000 microprocessor.

To provide your application compatibility with the SDK ARM64, you should follow the requirements described in the document written in Russian under the title «Базовый набор требований и рекомендаций по построению аппаратных платформ на базе СнК (SoC) BE-S1000» that is under development.

# Contact Info

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# Revision History

| Revision | Date | Substantive change(s) |
|---|---|---|
| 0.30 | December 13, 2021 | Initial version |
| 0.33 | March 17, 2022 | Added:<br>• Ordering Information<br>• Supported ISAs in Arm Cortex-A75 CPU Cluster |
| 0.35 | July 05, 2022 | Added:<br>• Packing<br>• Delivery Set<br>• Marking<br>• SDK<br>• Power Supply Requirements<br>• Figure 4-1 Start Sequence Diagram for the BE-S1000 |
| 0.37 | January 16, 2023 | Minor edits |